

# JEDEC STANDARD

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**FBDIMM**

**Advanced Memory Buffer (AMB)**

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**JESD82-20A.01**

(Editorial Revision of JESD82-20A, March 2009)

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## FBDIMM: Advanced Memory Buffer (AMB)

(From JEDEC Board ballot JCB-06-42, formulated under the cognizance of the JC-40 Committee on Digital Logic.)

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### 1 Introduction

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This document is a core specification for a Fully Buffered DIMM (FBD) memory system. This document, along with the other core specifications, must be treated as a whole. Information critical to a Advanced Memory Buffer design appears in the other specifications, with specific cross-references provided.

#### 1.1 Advanced Memory Buffer Overview

The Advanced Memory Buffer (AMB) reference design complies with the *FB-DIMM Architecture and Protocol Specification*. It supports DDR2 SDRAM main memory. The Advanced Memory Buffer allows buffering of memory traffic to support large memory capacities. All memory control for the DRAM resides in the host, including memory request initiation, timing, refresh, scrubbing, sparing, configuration access, and power management. The Advanced Memory Buffer interface is responsible for handling FBD channel and memory requests to and from the local DIMM and for forwarding requests to other DIMMs on the FBD channel.

Fully Buffered DIMM (FBD) provides a high memory bandwidth, large capacity channel solution that has a narrow host interface. Fully Buffered DIMMs use commodity DRAMs isolated from the channel behind a buffer on the DIMM. The memory capacity is 288 devices per channel and total memory capacity scales with DRAM bit density. The Advanced Memory Buffer is the buffer that isolates the DRAMs from the channel.

#### 1.2 Advanced Memory Buffer Functionality

##### 1.2.1 Advanced Memory Buffer

The Advanced Memory Buffer will perform the following FBD channel functions:

- Supports channel initialization procedures as defined in the initialization chapter of the *FB-DIMM Architecture and Protocol Specification* to align the clocks and the frame boundaries, verify channel connectivity, and identify AMB DIMM position.
- Supports the forwarding of southbound and northbound frames, servicing requests directed to a specific AMB or DIMM, as defined in the protocol chapter, and merging the return data into the northbound frames.
- If the AMB resides on the last DIMM in the channel, the AMB initializes northbound frames.
- Detects errors on the channel and reports them to the host memory controller.
- Support the FBD configuration register set as defined in the register chapters.
- Acts as DRAM memory buffer for all read, write, and configuration accesses addressed to the DIMM.
- Provides a read buffer FIFO and a write buffer FIFO.
- Supports an SMBus protocol interface for access to the AMB configuration registers.
- Provides logic to support MEMBIST and IBIST Design for Test functions.
- Provides a register interface for the thermal sensor and status indicator.
- Functions as a repeater to extend the maximum length of FBD Links.

### **1.2.2 Transparent Mode for DRAM Test Support**

In this mode, the Advanced Memory Buffer will provide lower speed tester access to DRAM pins through the FBD I/O pins. This allows the tester to send an arbitrary test pattern to the DRAMs. Transparent mode only supports a maximum DRAM frequency equivalent to DDR2 400.

Transparent mode functionality:

- Reconfigures FBD inputs from differential high speed link receivers to two single ended lower speed receivers (~200 MHz)
- These inputs directly control DDR2 Command/Address and input data that is replicated to all DRAMs
- Uses low speed direct drive FBD outputs to bypass high speed Parallel/Serial circuitry and provide test results back to tester

### **1.2.3 Debug and Logic Analyzer Interface**

When optional LAI functionality is supported, the Advanced Memory Buffer can be used to support the connection of FBD links to a Logic Analyzer (LA) for debug.

Advanced Memory Buffer debug functionality:

- Reconfigures DDR2 interface to act as a Logic Analyzer Interface (LAI) to observe activity on FBD high speed links
- Triggers on programmable events in normal operation

### **1.2.4 DDR SDRAM**

DDR2 SDRAM support:

- Supports DDR2 at speeds of 533, 667, and 800 MT/s
- Supports 256, 512, 1024, 2048, and 4096 Mb devices in x4 and x8 configurations
- 288 devices/channel (8 DIMMs/channel, 1 and 2 ranks/DIMM)
- 72-bit DDR2 SDRAM unregistered, unbuffered memory interface

1.3 Advanced Memory Buffer Block Diagram

Figure 1 is a conceptual block diagram of the Advanced Memory Buffer’s data flow and clock domains.

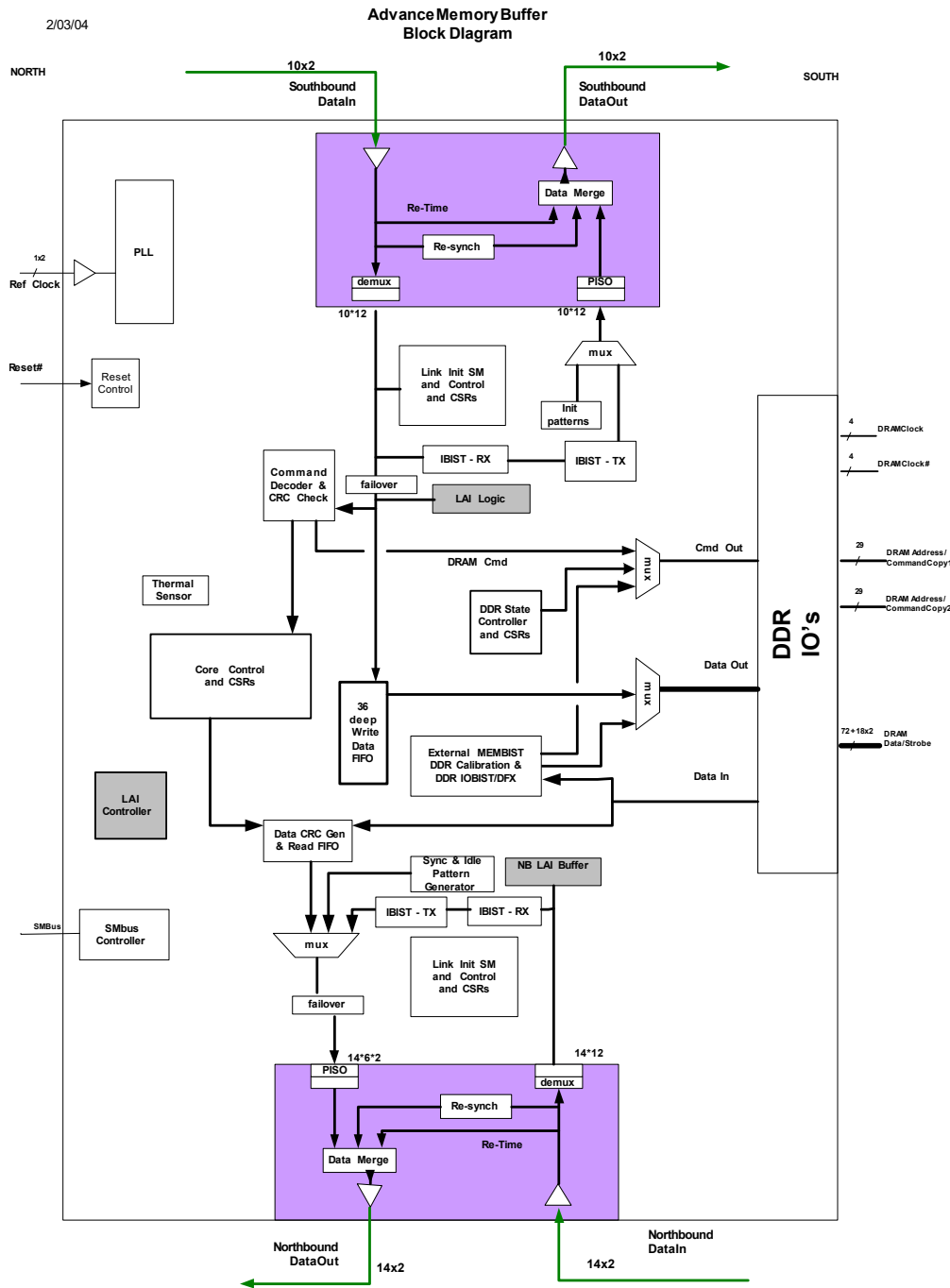
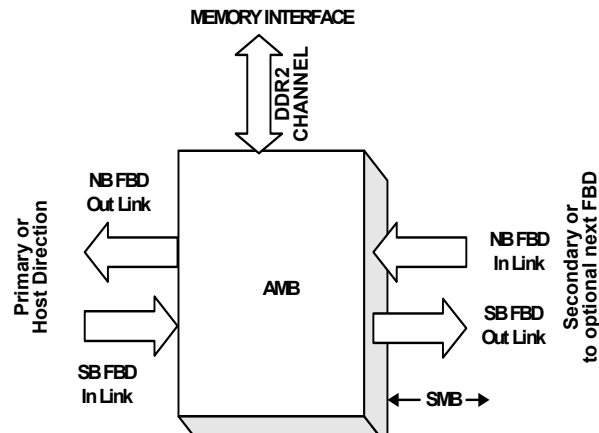


Figure 1 — Advanced Memory Buffer Block Diagram

## 1.4 Interfaces

Figure 2 illustrates the Advanced Memory Buffer and all of its interfaces. They consist of two FBD links, one DDR2 channel and an SMBus interface. Each FBD link connects the Advanced Memory Buffer to a host memory controller or an adjacent FBD. The DDR2 channel supports direct connection to the DDR2 SDRAMs on a Fully Buffered DIMM.



**Figure 2 — Advanced Memory Buffer Interfaces**

### 1.4.1 FBD High-Speed Differential Point-to-Point Link (at 1.5 V) Interfaces

The Advanced Memory Buffer supports one FBD Channel consisting of two bidirectional link interfaces using high-speed differential point-to-point electrical signaling.

The southbound input link is 10 lanes wide and carries commands and write data from the host memory controller or the adjacent DIMM in the host direction. The southbound output link forwards this same data to the next FBD.

The northbound input link is 13 to 14 lanes wide and carries read return data or status information from the next FB DIMM in the chain back towards the host. The northbound output link forwards this information back towards the host and multiplexes in any read return data or status information that is generated internally.

### 1.4.2 DDR2 Channel

The DDR2 channel on the Advanced Memory Buffer supports direct connection to DDR2 SDRAMs. The DDR2 channel supports two ranks of eight banks with 16 row/column request, 64 data signals, and eight check-bit signals. There are two copies of address and command signals to support DIMM routing and electrical requirements. Four-transfer bursts are driven on the data and check-bit lines at 800 MHz.

Propagation delays between read data/check-bit strobe lanes on a given channel can differ. Each strobe can be calibrated by hardware state machines using write/read trial and error (or equivalent implementation). Hardware aligns the read data and check-bits to a single core clock.

The Advanced Memory Buffer provides four copies of the command clock phase references (CLK[3:0]) and write data/check-bit strobes (DQSs) for each DRAM nibble.



## 1.4 Interfaces (cont'd)

### 1.4.3 SMBus Target Interface

The Advanced Memory Buffer supports an SMBus interface to allow system access to configuration registers independent of the FBD link. The Advanced Memory Buffer will never be a controller on the SMBus, only a target. Serial SMBus data transfer is supported at 100 kHz.

SMBus access to the Advanced Memory Buffer may be a requirement to boot a system. This provides a mechanism to set link strength, frequency and other parameters needed to insure robust operation given platform specific configurations. It is also required for diagnostic support when the link is down.

The SMBus address straps located on the DIMM connector are used by the Advanced Memory Buffer to get its unique ID.

More information is available in the SMBus chapter of this document.

## 1.5 References

This revision of the *Advanced Memory Buffer Component Specification* is consistent with the following documents:

- *FB DIMM Architecture and Protocol Specification*, [1]
- *FBD Design for Test, Design for Validation (DFx) Specification*, [2]
- *FB4300/5300/6400 DDR2 Fully Buffered DIMM Design Specification*, [3]
- *JEDEC DDR2 SDRAM Specification*, JC 42.3 [4]
- *High Speed Differential Point-to-Point Link at 1.5 V for Fully Buffered DIMM*, [5]
- *System Management Bus (SMBus) Specification Version 2.0 as published by www.smbus.org* [6]
- *Advanced Configuration and Power Interface Specification Version 2.0c as published by www.acpi.info* [7]

## 1.6 Glossary

**Glossary Table**

Term	Definition
AMB	Advanced Memory Buffer
Chip disable	An ECC encoding specifically tailored for memory such that the data from any defective memory device can be reconstructed from some aggregate of surviving memory devices. Corrects data from failed device. The AMB employs an “x8” ECC, which means that all data from a partially or completely failed 8-bit device can be recovered without stopping the system. This same ECC provides the same level of coverage for 4-bit (“x4”) devices.
DDR	Double Data Rate (SDRAM)
DDR Branch	The minimum aggregation of DDR channels which operate in lock-step to support error correction. Two channels per branch supports x8 chip disable ECC. A rank spans a branch.
DDR Channel	A DDR channel consists of a data channel with 72 bits of data and an ADDR/CNTRL channel
DDR Data channel	A DDR data channel consists of 72 bits of data, divided into 18 data groups
DDR Data group	Each data group consists of 4 data signals and a differential strobe pair

**Glossary Table (Continued)**

<b>Term</b>	<b>Definition</b>
DIMM	Dual In-Line Memory Module. A packaging arrangement of memory devices on a socketable substrate.
DIMM Slot	Receptacle (socket) for a DIMM. Also, the relative physical location of a specific DIMM on a DDR channel.
DIMM Stack	Dual-ranked x4 DRAM DIMM physical topology: refers to two physical rows of DRAM “stacked” one above another
DRAM Page (Row)	The DRAM cells selected by the Row Address
DPM	Defects per million
DRAM	Dynamic Random Access Memory
ECC	Error Correction Code. For the AMB, this is a chip disable code.
EMI	Electromagnetic interference
FBD Channel	Combination of 10 lane Southbound Links and 13 or 14 lane Northbound Links that make up a logical memory channel from host perspective
FBDIMM	Fully-Buffered DIMM
Frame	Group of bits containing commands or data
HCSL	High-speed Current Steering Logic
Host	Memory controller agent on an FBD channel
ISI	Inter Symbol Interference – see section “Initialization / Clocking” for definition
Mesochronous	Small ppm frequency difference.
NB	North Bound
NBI	North Bound Interface control logic
Northbound	The direction of signals running from the furthest DIMM toward the host.
JEDEC	JEDEC Solid State Technology Association (once known as the Joint Electron Device Engineering Council)
JESD79	JEDEC Standard 79, <i>DDR SDRAM Specification</i>
LA	Logic Analyzer
LAI	Logic Analyzer Interface
Lane	Differential pair of receivers or transmitters
Link	High speed parallel Differential Point-to-Point interface
Page Replace aka Page Miss, Row Hit / Page Miss	An access to a row that has another page open. The page must be transferred back from the sense amps to the array, and the bank must be precharged.
Page Hit	An access to an open page, or DRAM row. The data can be supplied from the sense amps at low latency.
Page Miss (Empty Page)	An access to a page that is not buffered in sense amps and must be fetched from DRAM array.
Plesiochronous	Having the same frequency but arbitrary phase differences.
Primary	In the direction towards the Host controller
PLL	Phase Locked Loop

**Glossary Table (Continued)**

<b>Term</b>	<b>Definition</b>
PTH	Plated Through-Hole
PVT	Process, Voltage and Temperature
Rank	A DIMM is organized as one or two physical sets of memory, called ranks. Note that single rank or dual rank is different from single-sided or double-sided, e.g., a single rank DIMM build from x4 DRAM devices is actually double-sided. It is also common practice to distribute the 9 devices of an x8 DIMM between both sides of the DIMM to enhance the thermal performance of the module. The standard 4-slot DDR2 topology is limited to single rank DIMM due to loading constraints.
RAS	Reliability, Availability, Serviceability
Resample	A resampler is a serial data in and serial data out node that attenuates jitter by regenerating the serial data using a clock recovered from the incoming data stream derived from a common reference clock. It also resets the voltage budget of the retransmitted data.
Resync	A resync repeater is a serial data in and serial data out node that resynchronizes data to a local clock after it has been sampled with a recovered clock derived from a common reference clock. The local clock is also generated from the same reference clock by a PLL multiplier. A drift compensation buffer is inserted between the two clock domains which absorbs the maximum link delay change over worst case voltage and temperature changes only, and not for compensating lane-to-lane skew. Both the jitter and voltage budgets for the retransmitted data are reset.
RPD	Return Path Discontinuity
SDRAM	Synchronous Dynamic Random Access Memory
SB	South Bound
SBI	South Bound Interface control logic
SI	Signal Integrity
Secondary	In the direction away from the Host controller
Serial Present Detect (aka SMBus protocol)	A 2-signal serial bus used to read and write control registers in the AMB and SDRAM
SMBus	System Management Bus. Controlled by a system management controller to read and write configuration registers. Limited to 100 kHz.
Southbound	The direction of signals running from the host controller toward the DIMMs.
SSC	Spread Spectrum Clocking. Utilized to lower EMI
SSO	Simultaneously Switching Outputs
SSTL_18	Series Stub Terminated Logic for 1.8 V
NB	North Bound
NBI	North Bound Interface control logic
Throttled	Temporarily prohibiting memory accesses when a thermal or electrical limit has been reached.
Transparent Mode	High speed FBD linked I/Os are bypassed with lower speed CMOS I/Os to allow lower speed tester to control and test DRAMs on the DIMM.

Glossary Table (Continued)

Term	Definition
Unit Interval	Average time interval between voltage transitions of a signal
V <sub>SS</sub>	Ground (0V)
V <sub>DDQ</sub>	I/O buffer voltage for DDR2 buffers. Nominally 1.8 V

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## 2 FBD Channel Interface

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### 2.1 Advanced Memory Buffer Support for FBD Operating Modes

The Advanced Memory Buffer (AMB) may not support all operating modes documented in the *FB-DIMM Architecture and Protocol Specification* [1]. The following list defines which features/modes are supported:

- 14 lane northbound (NB) with and without single lane Fail Over
- 13 lane NB with and without single lane Fail Over
- 10 lane southbound (SB) with and without single lane Fail Over
- Repeater mode
- Transparent mode
- Recalibrate state
- Voltage Margin Test

The following are optional FBD features :

- LAI mode
- 12 lane NB non-ECC
- L0s low power state
- Data mask
- Variable read latency
- Timing Margin Test

### 2.2 Channel Initialization

Refer to Chapter 3, “Channel Initialization” in the *FB DIMM Architecture and Protocol Specification* [1] for FBD initialization protocol. The reset chapter covers some additional details about the initialization process.

### 2.3 Channel Protocol

#### 2.3.1 General

Refer to Chapter 4, “Channel Protocol” in the *FB DIMM Architecture and Protocol Specification* [1] for FBD protocol.

#### 2.3.2 Timeouts during TS0

The FBDLOCKTO register is used to help the AMB determine when to give up waiting for individual lanes to bit lock. The NBLINKCFG field is used to communicate when lanes are intentionally not in use. The BLTOCNT field is used to set a time out on waiting for a lane to bit lock. Lanes not bit locked by this time will be marked as failed.

<b>Recal Frame Counter:</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
Rx Data <sup>1</sup>	X	X	X	NOP	NOP	Valid Cmd
NOTE 1 X represents “don’t care” data						

## 2.3 Channel Protocol (cont'd)

### 2.3.4 Address Mapping of DDR Commands to DRAMs

DDR2 x4 Config		20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
256Mb (64Mbx4)	Row	1	X	X	RS	X	X	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1KB page	Col	0	1	r/w	RS	X	X	B1	B0	X	A11	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
512Mb (128Mbx4)	Row	1	X	X	RS	A13	X	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1KB page	Col	0	1	r/w	RS	X	X	B1	B0	X	A11	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1Gb (256Mbx4)	Row	1	X	X	RS	A13	B2	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1KB page	Col	0	1	r/w	RS	X	B2	B1	B0	X	A11	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
2Gb (512Mbx4)	Row	1	X	A14	RS	A13	B2	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1KB page	Col	0	1	r/w	RS	X	B2	B1	B0	X	A11	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
4Gb (1Gbx4) *	Row	1	A15	A14	RS	A13	B2	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1KB page	Col	0	1	r/w	RS	X	B2	B1	B0	X	A11	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
4Gb (1Gbx4) *	Row	1	X	A14	RS	A13	B2	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
2KB page	Col	0	1	r/w	RS	X	B2	B1	B0	A12	A11	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
DDR2 x8 Config		20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
256Mb (32Mbx8)	Row	1	X	X	RS	X	X	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1KB page	Col	0	1	r/w	RS	X	X	B1	B0	X	X	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
512Mb (64Mbx8)	Row	1	X	X	RS	A13	X	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1KB page	Col	0	1	r/w	RS	X	X	B1	B0	X	X	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1Gb (128Mbx8)	Row	1	X	X	RS	A13	B2	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1KB page	Col	0	1	r/w	RS	X	B2	B1	B0	X	X	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
2Gb (256Mbx8)	Row	1	X	A14	RS	A13	B2	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1KB page	Col	0	1	r/w	RS	X	B2	B1	B0	X	X	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
4Gb (512Mbx8) *	Row	1	A15	A14	RS	A13	B2	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1KB page	Col	0	1	r/w	RS	X	B2	B1	B0	X	X	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
4Gb (512Mbx8) *	Row	1	X	A14	RS	A13	B2	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
2KB page	Col	0	1	r/w	RS	X	B2	B1	B0	X	A11	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

### 2.3.5 FBD L0s State

The L0s state provides a low latency power down state for the FBD channel. The L0s state will nominally last for 41 frame times such that no sync packets are missed. The actual amount of time is programmable in the AMB. Times greater than 41 frames are not supported at this time. The L0s state may be used when the memory controller is throttling, and producing no transfers.

The duration of the L0s state is pre-programmed into the MC and AMB registers, and is triggered by a sync command with the L0s command indicated. The basic sequence is:

#### L0 to L0s Transition

- MC issues L0s command in the SYNC command.
- The MC continues sending one additional command, which is a NOP.
- AMB must gate its inputs and stop accepting commands following the NOP. It need not accept and decode the NOP itself.
- Southbound output drivers and input receivers are disabled following the NOP. The turnoff may be staggered for power supply di/dt reduction.
- Northbound channels are shut down following the status packet corresponding to the sync command.
- AMB takes CKE low to all DRAMs and floats the commands and address bus to the DRAMS (all signals except clock, CKE, and ODT).
- The PLL is never powered down before, during, or after the transition.

## 2.3 Channel Protocol (cont'd)

### 2.3.5 FBD L0s State (cont'd)

#### L0s to L0 Transition

- When the timer expires, interface must be fully functional and ready to receive the sync command. The turning on of circuits occurs the proper amount of time prior to the timer expiring, and is an implementation detail of the AMB.
- Southbound channel begins power-up. The drivers must begin driving a valid state one clock prior to the NOP below.
- The AMB drives command and address lines, and restores CKEs to their previous state with appropriate timing to be able to process a DRAM command which is received on the clock following the sync command.
- MC sends a NOP on the clock prior to the timer expiring. The receiver need not accept and decode the NOP itself.
- MC sends a sync command on the clock that the timer expires.
- Normal commands may commence.
- Northbound lanes are brought back in a similar manner to southbound lanes, but are timed to be able to successfully send the status packet response for the sync command.

Note: DRAM pages need not be closed during the power down, but any DRAM with open pages will consume additional power. This is solely a function of the MC policy.

Note: Upon return to L0, the MC may place the bus back into L0s by issuing another L0s command in the sync command.

## 2.4 Reliability, Availability, and Serviceability

### 2.4.1 General

Refer to Chapter 5, “Reliability, Availability and Serviceability” in the *FB DIMM Architecture and Protocol Specification* [1] for FBD RAS requirements.

### 2.4.2 Channel Error Detection and Logging

See “Errors” chapter for details on the error handling.

## 2.5 Channel Configuration

### 2.5.1 Re-sync and Resample Modes

A separate control is available for both the NB and SB FBD links to select between lower latency re-sample and lower jitter re-sync modes for repeating received data. Selection between these two modes is a function of platform design and configuration and should be set by BIOS prior to link initialization

The FBDSBCFGNXT.SBRESYNCEN and FBDNBCFGNXT.NBRESYNCEN bits make this selection.

Descriptions of these two modes follows.



## 2.5 Channel Configuration (cont'd)

### 2.5.1.1 Accumulated Tracking Effects (Re-Sample Mode)

Each AMB acts as a repeater for the FBD channel. Since the data driven from each DIMM to the next DIMM may experience random or periodic phase shifts, the affect of these phase shifts must be accommodated in the design. Consider a system with three DIMMs daisy-chained together. A phase shift generated in the first DIMM will be seen by the second DIMM but will not be immediately propagated to the third DIMM. Unlike an analog buffer, the phase shift is not automatically driven to subsequent DIMMs since the data driven to the subsequent DIMMs is re-sampled in the AMB to reduce jitter. The lowest latency implementation would use the derived clock to retransmit the outbound signal. The second DIMM will see the phase shift as a slight change in the position of the data eye at its receiver. The clock tracking loop filter in the second DIMM will measure several bit cells and may eventually determine that it should adjust the phase of its derived clock to capture the data closer to the center of the new data eye location. Only when the second DIMM makes its phase change will the effect propagate to the third DIMM. More detail of the data sampling technique may be found in the “High Speed Differential Point-to-Point Link at 1.5V for Fully Buffered DIMM Specification”.

### 2.5.1.2 Accumulated Tracking Effects (Re-Sync Mode)

An alternative implementation would place a voltage/thermal (VT) drift compensation buffer between the receiver and the transmitter section of the AMB IO cell. The drift compensation buffer would re-synchronize the signal with a multiple of the reference clock. This buffer would have to be deep enough to handle the absolute magnitude of delay change of the daisy-chain channel over voltage and temperature. More detail of the data sampling technique may be found in the “High Speed Differential Point-to-Point Link at 1.5V for Fully Buffered DIMM Specification”.

## 2.5.2 Other Channel Configuration Modes

Other channel electrical configuration parameters that should be set up prior to link initialization include

- Link frequency (LINKPARNXT.CFREQ)
- SB Transmitter drive current (FBDSBCFGNXT.SBTXDRVCUR)
- SB Transmitter de-emphasis values (FBDSBCFGNXT.SBTXPREEMP)
- NB Transmitter drive current (FBDNBCFGNXT.NBTXDRVCUR)
- NB Transmitter de-emphasis values (FBDNBCFGNXT.NBTXPREEMP)

The parameters contained in these registers are described more completely in the “High Speed Differential Point-to-Point Link at 1.5V for Fully Buffered DIMM Specification”.

Additional channel configuration registers that should be set up prior to link initialization include

- First 6 bytes of the SPD parameter registers  
PERSBYTE[5:0]
- FBD Bit Lock Time Out Register (FBDLOCKTO)

## 2.5.3 Lane to Lane Skew on a Channel

The FBD Channel is expected to support a maximum skew of upto 46UI. The deskew buffers on an individual AMB need to be able to support this amount of accumulated skew. The actual skew observed will be a function of the skew introduced by platform layout, DIMM layout, the number of active AMBs in the channel and skew introduced by AMBs.

## 2.6 Repeater Mode

The AMB may also be used as an FBD link repeater to extend distances at which links can operate. This mode can be automatically set by the BFUNC and SA pins. In this mode, the AMB functions in the same way as a regular DIMM with the exception that DRAM commands are not supported.

Link behavior is the same as for normal DIMMs

- Participates in link initialization like a normal DIMM
- Responds to Reads and Writes to AMB configuration registers,
- status is returned in response to Sync commands,
- link errors are detected and alerts generated,

SMBus access is the same except for the base Target address is different than from normal DIMM.

Target address[6:3] = 4'b0011 for Repeaters, instead of

Target address[6:3] == 4'b1011 for normal DIMMs

## 2.7 Performance

This section describes the performance characteristics of FBD: idle memory read latencies, loaded memory read latencies, channel throughput, and system memory capacity.

### 2.7.1 Idle Memory Read Latency

Memory read latency is an important factor in system level performance. Processor and I/O devices are often blocked from doing other work when reading from memory, until their read requests are satisfied. Therefore, minimizing the amount of time that it takes to satisfy a read request can increase the amount of work that a processor or I/O device can perform. This can improve overall system or benchmark performance.

Memory read latency (also referred as loaded memory read latency) consists of two components: idle memory read latency and queuing delays for various resources such as the front-side bus, memory controller queues, etc. Idle memory read latency is the latency of only one transaction running in the entire system, and is the least amount of latency that is possible for a read transaction. The following sections describe how to measure the FBD channel latency, as well as the overall system latency.

#### 2.7.1.1 FBD Channel Latency

FBD channel latency is measured from the time a read request is driven on the FBD channel pins to the time when the first 16 bytes (2nd chunk) of read completion data is sampled by the memory controller.

When not using the Variable Read Latency capability, the latency for a specific FBD DIMM on an FBD channel is always equal to the latency for any other FBD DIMM on that channel. However, the latency for each FBD DIMM in a specific configuration with some number of FBD DIMMs installed may not be equal to the latency for each FBD DIMM in a configuration with some different number of FBD DIMMs installed.

As more DIMMs are added to the FBD channel, additional latency is required to read from each DIMM on the channel. Because the FBD channel is based on the point-to-point interconnection of buffer components between DIMMs, memory requests are required to travel through N-1 buffers before reaching the Nth buffer. The result is that a 4 DIMM channel configuration will have greater idle read latency compared to a 1 DIMM channel configuration.

The Variable Read Latency capability can be used to reduce latency for DIMMs closer to the host.

The idle latencies listed in this section are representative of what might be achieved in typical AMB designs. Actual implementations with latencies less than the values listed will have higher application performance and vice versa.

## 2.7.1 Idle Memory Read Latency (cont'd)

### 2.7.1.1 FBD Channel Latency (cont'd)

The following table shows typical idle read latency, using DDR2 667 (4-4-4) DRAM technology (for a page empty read). Actual values depend on platform board and DIMM routing, AMB timing specs, DRAM characteristics. etc.

**Table 1 — Example FBD-667 Channel Idle Memory Read Latencies**

DIMMs per Channel	Typical Latencies
1	43-47 ns
2	49-53 ns
3	52-56 ns
4	58-62 ns

Table assumptions:

- Measure from latest valid SB output pin at host to latest valid NB input pin at host
- Includes 4UI serialization delay SB (A slot command) and 12 UI serialization delay NB
- Routing delay of 850ps from host to first DIMM and 600ps DIMM to DIMM
- 4-4-4 SDRAM Access Timing (24ns) plus 400ps Tdqsk
- On-DIMM Clk and DQS propagation delays of 800ps
- FBD SB Cmd In to DDR Clk out that Latches Cmd Out of 8.1ns +/- 1ns
- DDR Read Data In to FBD NB Out (last DIMM) of 5ns +/- 1ns
- Resample cross AMB delays of 1.25ns and Resync pass thru delays of 2.25ns
- First AMB in Resync and other AMBs in Resample mode

## 2.8 AMB Components of Channel Latency

The critical elements that AMB contributes to the latency calculation are the chip crossing delays.

- Southbound latency contributions
  - Delay from an input FBD link transaction to commands on the DDR interface and
  - Pass-thru delay of forwarded Southbound FBD transactions.
- Northbound latency contributions
  - Delay from DDR Read data input on the last DIMM to FBD link transactions and
  - Pass-thru delay of forwarded Northbound FBD transactions back towards the host.

These timing delay values are documented in Chapter 4, “Electrical, Power, and Thermal.”

### 2.8.1 Command to Data Delay Calculation

The diagram illustrates the timing of a read operation across several components: SB (System Buffer), DDR (Double Data Rate), DRAMs (Dynamic Random Access Memory), and NB (North Bridge). The sequence of events is as follows:

- SB Frame Clock**: The initial clock signal for the system buffer.
- DDR Command**: The command signal sent to the DDR controller.
- DDR IO CMD Clock**: The clock signal for the DDR IO command.
- DRAM Clock**: The clock signal for the DRAMs.
- DRAMs**: The memory array where data is read.
- Data**: The data signal sent from the DRAMs to the NB.
- DQS**: The data strobe signal sent from the DRAMs to the NB.
- NB Frame Clock**: The clock signal for the north bridge.

Key timing parameters are indicated by arrows and labels:

- $T_{AMB\_Cmd\_Delay}$ : Delay from SB Frame Clock to DDR Command.
- $T_{Dimm\_Cmd\_Delay}$ : Delay from DDR Command to DRAM Clock.
- $T_{Read\_Latency}$ : Delay from DRAM Clock to Data/DQS.
- $T_{Dimm\_Data\_Delay}$ : Delay from Data/DQS to NB Frame Clock.
- $T_{AMB\_Data\_Delay}$ : Delay from NB Frame Clock to the final output.

### Figure 3 — Delays Through an AMB

- UI: This is the unit interval on the FBD link. This is same as the period of the FBD link bit-rate clock.
- NB: Northbound
- SB: Southbound
- $T_{\text{Read\_Latency}}$ : DRAM Parameter.  $T_{\text{CAS}} + T_{\text{Additive\_Latency}}$
- $T_{\text{AMB\_Cmd\_Delay}}$ : This value is very specific to an AMB implementation. This is the time it takes for the FBD command to be transferred from the point at which a deskewed and frame aligned command is available to core to the DDR IO Cluster. This includes any differences between the FBD frame clock and the DDR IO clock that latches the command into the DDR IO cluster. This can be different for different DRAM frequencies.
- $T_{\text{AMB\_Data\_Delay}}$ : This value is very specific to an AMB implementation. This is the minimum time it takes for the data that is returned from the DRAMs to be transferred from the DDR IO cluster to the FBD IO for transmission on the link. This includes any buffering and clocking delays for the data within the chip. This can be different for different DRAM frequencies.
- $T_{\text{Dimm\_Cmd\_Delay}}$ : This includes the delays for the command through the DDR IO cluster, differences between DDR IO CMD Clock and DRAM clock, any routing delays for the clock and command on the DIMM and any set-up and hold-times in the AMB and the DRAMs.

## 2.8 AMB Components of Channel Latency (cont'd)

### 2.8.1 Command to Data Delay Calculation (cont'd)

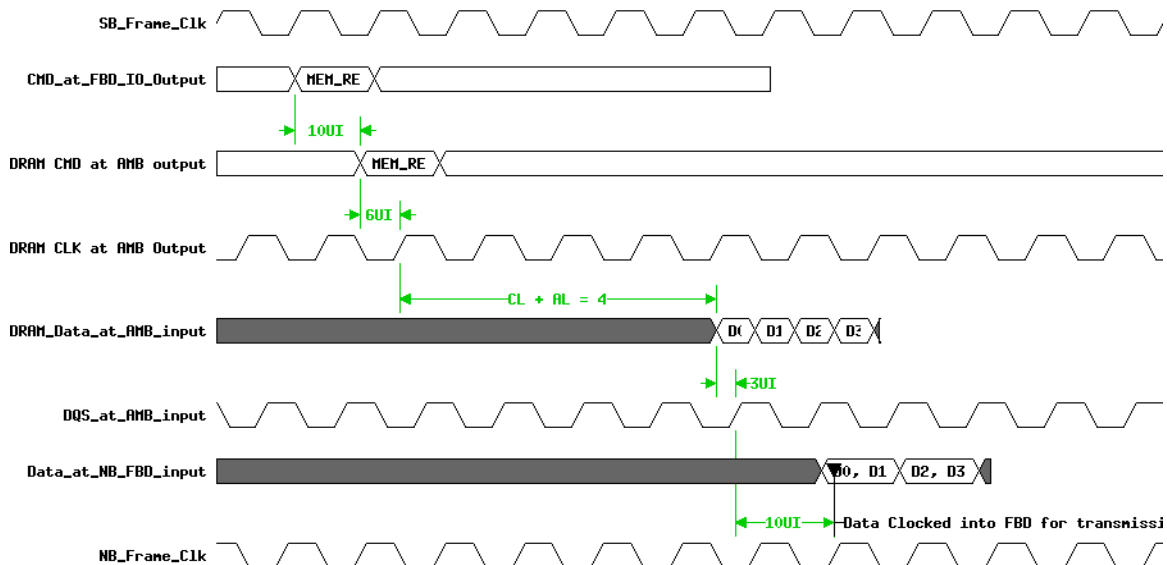
- $T_{\text{Dimm\_Data\_Delay}}$ : This includes the routing delays for the data and strobes from the DRAM to the AMB, skews between the DRAMs, delays through the DDR IO cluster and any set-up and hold-times in the AMB and DRAMs.
- $T_{\text{CMD\_To\_Data}}$ : This is equal to  $(T_{\text{Read\_Latency}} + T_{\text{AMB\_Cmd\_Delay}} + T_{\text{Dimm\_Cmd\_Delay}} + T_{\text{Dimm\_Data\_Delay}} + T_{\text{AMB\_Data\_Delay}})$ . This can be specified with 1UI granularity. This will be different for each DRAM type. It does not include any delays inside the IO to deskew and frame align the incoming data on the SB side nor does it include the delays inside the NB IO on the transmit side.

The TCAS and TAdditive\_Latency are specified in the DRC register (DRC.cl and DRC.al). The AL and CL values are latched from the DRC register during TS2's to establish TRead\_Latency. Later changes to AL and CL do not take effect for link data return timing until the next link reset.

The CMD2DATANXT register is initialized with a value equal to  $(T_{\text{CMD\_To\_Data}} - T_{\text{Read\_Latency}})$ . This value of CMD2DATANXT is specified in the SPD EEPROM. All AMBs are expected to receive the data from the DRAMs with the calculated value of  $T_{\text{CMD\_To\_Data}}$ .

All AMBs power up with a default value of 5 for  $T_{\text{CMD\_To\_Data}}$ . This can be done either by setting the default values of DRC.CL and DRC.AL or by setting the default value of the CMD2DATACUR.FRMS to be 5. The AMBs must be able to return status and configuration register reads with this default timing. This will enable the BIOS to initialize the proper values from SPD.

The following simplified timing diagram illustrates how the last AMB uses the values specified in DRC.CL, DRC.AL, CMD2DATANXT.DLYFRMS and CMD2DATANXT.DLYFRAC.



**Figure 4 — Command to Data Delay Timing**

In Figure , it is assumed that there are no routing delays on the DIMM itself. The command takes 10UI to get from SB FBD to the DDR IO ( $T_{\text{AMB\_Cmd\_Delay}}$ ). This includes time it takes to validate CRC of the frame and to decode the command. It is assumed  $\text{DDR\_IO\_Cmd\_Clk}$  shown in Figure is delayed from the  $\text{SB\_Frame\_Clk}$  by 10 UI. The DRAM SCLK is placed at the center of the command window which adds an additional 6UI of delay. The DRAMs are programmed with a  $T_{\text{Read\_Latency}}$  of 4.

## 2.8 AMB Components of Channel Latency (cont'd)

### 2.8.1 Command to Data Delay Calculation (cont'd)

The DQS strobes are centered when they get to the AMB (3UI delay) and the data takes an additional 10 UI to propagate from the DDR IO to the NB FBD IO (including setup time at NB FBD and CRC generation) before it can be clocked into the NB FBD for transmission. The total delay without including the DRAM access time in this case is  $(10 + 6 + 3 + 10\text{UI})$  29UI. The CMD2DATANXT.DLYFRMS will be programmed with a value 2 and the CMD2DATANXT.DLYFRAC with 5UI. If the AMB supports only a 2UI granularity, then the values should be 2 frames and 6UI respectively. If an AMB does not support sub-frame delays, it is expected that the value in SPD will be round up to the nearest frame. Any additional delays caused by rounding up should be supported by additional buffering in the DDR IO.

The above figure shows the last arriving data from the DDR. It is expected that any data arriving earlier than this, due to differences in routing, etc. is buffered up in some way inside the DDR IO. The expectation is that all AMBs (last and intermediate) unload the data from the DDR IO with the timing specified by the  $T_{\text{CMD To DATA}}$ . The Last AMB is expected to be able send data on the NB links with no additional delay added, if C2DINRCUR.INCRDLY is 0. Any additional delay needed due to the value programmed in C2DINRCUR.INCRDLY register in the last AMB or to delay the data in intermediate AMB before the merge, is handled by FIFOs in the AMB core.

In the above figure, it is assumed that the AMB can place the clocks in position shown above. If this is not the case, then additional delays due to non-optimal placement of the clocks should be taken into account to calculate the total delay to be programmed into the SPD.

## 2.8.2 Channel Throughput

### 2.8.2.1 Peak Theoretical Throughput

An FBD channel transfers read completion data on the FBD Northbound data connection. 144 bits of data are transferred for every FBD Northbound data frame. This matches the 18-byte data transfer of an ECC DDR DRAM in a single DRAM command clock. A DRAM burst of 8 from a single channel or a DRAM burst of four from two lock-stepped channels provides a total of 72 bytes of data (64 bytes plus 8 bytes ECC).

The FBD frame rate matches the DRAM command clock because of the fixed 6:1 ratio of the FBD channel clock to the DRAM command clock. Therefore, the Northbound data connection will exhibit the same peak theoretical throughput as a single DRAM channel. For example, when using DDR2 533 DRAMs, the peak theoretical bandwidth of the Northbound data connection is 4.267 GB/sec.

Write data is transferred on the FBD Southbound command and data connection, via Command+Wdata frames. 72 bits of data are transferred for every FBD Command+Wdata frame. Two Command+Wdata frames match the 18-byte data transfer of an ECC DDR DRAM in a single DRAM command clock. A DRAM burst of 8 transfers from a single channel, or a burst of 4 from two lock-step channels provides a total of 72 bytes of data (64 bytes plus 8 bytes ECC).

When the FBD frame rate matches the DRAM command clock, the Southbound command and data connection will exhibit one half the peak theoretical throughput of a single DRAM channel. For example, when using DDR2 533 DRAMs, the peak theoretical bandwidth of the Southbound command and data connection is 2.133 GB/sec.

The total peak theoretical throughput for a single FBD channel is defined as the sum of the peak theoretical throughput of the Northbound data connection and the Southbound command and data connection. When the FBD frame rate matches the DRAM command clock, this is equal to 1.5 times the peak theoretical throughput of a single DRAM channel. For example, when using DDR2 533 DRAMs, the peak theoretical throughput of a DDR2 533 channel would be 4.267 GB/sec, while the peak theoretical throughput of an FBD-533 channel would be 6.4 GB/sec.

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## 3 DDR Interface

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### 3.1 Advanced Memory Buffer DDR Interface Overview

The DDR interface on the Advanced Memory Buffer consists of:

- A command decoder.
- A FIFO write buffer to hold the write data before it is written to the DDR channel. The write FIFO buffer has 36 entries of 72 bits (36 x 72b). A maximum of 35 entries can be used to store DDR bursts. Write data targeted for other Advanced Memory Buffer parts on the channel will use three of the 35 entries until the target Advanced Memory Buffer is known. The write FIFO buffer fills at half of the DDR data rate, and empties at the DDR data rate. The write FIFO buffer must support an invalidate write FIFO command (FBD Soft Reset command).
- A FIFO read buffer to hold the read data so that each DIMM returns data with the same latency as the southernmost DIMM in the chain. Latency is measured in increments of core clock periods. The core clock runs at the DDR command clock rate (half the data rate frequency). The latency through the FIFO read buffer on the southernmost DIMM is expected to be zero.
- A DDR cluster which serves as a DIMM buffer by registering outbound commands and data at output flops. The cluster also captures and levelizes incoming read data.
- A reset FSM which puts the DIMM in self-refresh when reset is asserted, and exits self-refresh when reset is deasserted and southbound frame training is complete.
- A calibration FSM that automatically sets the timing for DQS receiver enable and DQS delay or equivalent DDR timing control mechanism.
- A configuration register set to allow software to issue DRAM power up and DRAM MRS/EMRS commands. These registers are accessible through FBD channel commands and the SMBUS interface.
- "Burst Write Interrupt" is not supported.

### 3.2 Data Mapping

See the protocol chapter of the *FB DIMM Architecture and Protocol Specification* for the mapping between data in DDR DRAM devices and data in FBD frame formats for 4-bit and 8-bit devices.

#### 3.2.1 Data Mask

Data mask is supported for non-ECC (64-bit) DIMMs only. The AMB is required to support data mask if it supports non-ECC DIMMs.

Non-ECC DIMMs using x4 DRAMs are not supported by the standard AMB pinout, as there are not adequate data mask pins available. 16 data mask pins would be required for proper load matching.

The data mask signals share pins with the DQS[16:9] pins. This puts them in the proper place on the package and die to be matched with the timing of the appropriate DQ pins. DQS#[16:9] are not used in this mode. The following table shows the mapping between DQS pins and data mask pins.

## 3.2 Data Mapping (cont'd)

### 3.2.1 Data Mask (cont'd)

Data Lane	Signal	x4 Usage	Non-ECC Usage	x8 or x16 ECC Usage
DQ[7:0]	DQS[9]/DM0	DQS[9]	DM0	Not used
DQ[15:8]	DQS[10]/DM1	DQS[10]	DM1	Not used
DQ[23:16]	DQS[11]/DM2	DQS[11]	DM2	Not used
DQ[31:17]	DQS[12]/DM3	DQS[12]	DM3	Not used
DQ[39:32]	DQS[13]/DM4	DQS[13]	DM4	Not used
DQ[47:40]	DQS[14]/DM5	DQS[14]	DM5	Not used
DQ[55:48]	DQS[15]/DM6	DQS[15]	DM6	Not used
DQ[63:56]	DQS[16]/DM7	DQS[16]	DM7	Not used
DQ[71:64]	DQS[17]	DQS[17]	Not used	Not used
As above	DQS[17:9]#	DQS[17:9]#	Not used	Not used

An AMB in non-ECC mode implies the following:

- 12 lane Northbound mode
- There is no Northbound fail-over mechanism.
- Data Mask Capability.
- Southbound write data frames use the Data Mask version of the frame format.
- 10 lane Southbound with fail-over capability.
- x4 DRAMs are not supported by the standard AMB pinout.

For AMB silicon that supports both ECC and non-ECC modes, there is no strapping signal to indicate which DIMM type it is installed on. The AMB will use the information in the configuration state, transferred from the host in the TS3 packet to determine ECC or non-ECC mode. If programmed for 12-bit northbound mode non-ECC mode is used. If programmed into 14-bit, 14-bit Fail Over, 13-bit, or 13-bit Fail Over modes, ECC mode is used. The host will determine the type of DIMM by reading the SPD.

## 3.3 Command / Address Outputs

The DDR2 command and address signals are terminated to 0.9V on the DIMM. In order to reduce power, this termination is performed using series resistors to a V<sub>tt</sub> power supply, which is generated by voltage regulators on the system board and provided to the DIMM via connector pins. This power supply must be capable of sourcing and sinking current.

Two sets, or copies, of DRAM command and address output pins are provided for loading and timing considerations. Each set drives the same DRAM commands, but the two address busses are inverted from each other in order to reduce power consumption and heat produced on the DIMM. The command and address output pin behavior is detailed as follows:

1. Minimum address toggling. The address associated with the last command issued on the DRAM bus is retained during DRAM NOP/Deselect commands. The address and bank bits do not revert to all 1's (or all 0's) when the command bus is idle.



### 3.3 Command / Address Outputs (cont'd)

2. Balanced bank and address busses. With some exceptions, the bank and address busses on the two bus copies are inverted from each other. This minimizes the current load on the  $V_{TT}$  supply regulator because the balanced address bus sinks as much current as it sources. There are exceptions to the inversion behavior to allow for commands that use one or more address bits to control DRAM functionality. Balancing can also be disabled by setting the DRC.BALDIS register field.

Balancing Exceptions:

- a. Address bit A10 is not balanced during all read, write, and precharge commands.
  - b. No address or bank bits are balanced during any MRS and EMRS commands.
  - c. Some MEMBIST operations that are pattern specific. Note that this will limit the number of DIMMs that may run MEMBIST simultaneously.
  - d. No address or bank bits are balanced during any command when the DRC.BALDIS register field is set.
3. Balanced idle command bus. When the command bus is idle, a deselect command is issued with all chip selects high and all RAS/CAS/WE signals driven low on both command/address copies.
  4. Command/Address output control with CKE. All command and address pin outputs, except for ODT, CKE, and CLK, will float one DRAM clock cycle after both CKE pins transition from high to low. The command/address pins will be driven to valid signal levels on the same cycle that either CKE pin is driven from low to high.
  5. Output control during link reset (i.e., fast reset). When the Advanced Memory Buffer core logic is in reset, CKE and ODT will be driven low, and CLK will run at normal levels and frequency. The remaining command/address pins will float during reset.
  6. Command/Address output control in S3 mode. When the Advanced Memory Buffer core logic is in S3 power mode, CKE and ODT will be driven low. CLK and all the other command/address pins can be either driven low or tri-stated. In S3 mode, 1.8V supply is on. 1.5V and V<sub>tt</sub> supplies are off. 3.3V supply can be either on or off depending on user's design. DRAMs are in self refresh, and the CKE signals must be driven low.
  7. CSR output control of command/address. All command/address pin outputs will float when the appropriate DRC bits are set. Setting the DRC.CADIS field will float the RAS, CAS, WE, Bank, and Address pins. DRC.CSDIS controls the chip select pins. DRC.ODTDIS, DRC.CKEDIS, and DRC.CLKDIS float the ODT, CKE, and clock pins respectively.

#### 3.3.1 CKE Output Control

During normal operation the CKE outputs can be controlled directly with dedicated FBD channel commands and with configuration register writes to the DRC.CKEN0/1 CSR's. Channel commands that affect the CKE outputs are reflected in the DRC.CKEN0/1 CSR's. During channel fast reset events the self-refresh FSM controls the CKE outputs, as well as all other command/address outputs.

#### 3.3.2 Memory Controller / BIOS requirements

The memory controller must take care to not issue multiple MRS/EMRS commands to multiple DIMMs simultaneously in rapid succession if the V<sub>tt</sub> supply cannot handle the current.

The memory controller may also be required to limit the number of DIMMs in MEMBIST mode at the same time. V<sub>dd</sub> power supply and thermal limitations may also put a limit on how many DIMMs may be in MEMBIST at one time. These will be system dependent.

### 3.4 DQS IO and DM Outputs

Advanced Memory Buffer sends and receives source synchronous differential strobes (DQS) to transfer data (DQ/CB) during write and read DRAM transactions. DQS9 through DQS17 also support the data mask (DM) function in x8 mode. Setting the MTR.WIDTH configuration register enables x8 mode. When driving DM, the timing of the transition from floating, to driving, and back to floating is unchanged, but DQS[17:9] do not toggle and instead drive a constant level. DQSP[17:9] drive low and DQSN[17:9] drive high. In x8 mode DQS[17:9] are not used to capture read data. The table below lists which DQS signals are associated with which DQ/CB pins in x8 and x4 mode.

**Table 2 — DQS Association with DQ/CB Pins in x8 and x4 Mode**

DQS pin	x4 Mode: MTR.WIDTH=0		x8 Mode: MTR.WIDTH=1	
	Output Function	Input/Output Data Mapping	Output Function	Input/Output Data Mapping
DQS17	Write DQS	CB[7:4]	DM	N/A
DQS8	Write DQS	CB[3:0]	Write DQS	CB[7:0]
DQS16	Write DQS	DQ[63:60]	DM	N/A
DQS7	Write DQS	DQ[59:56]	Write DQS	DQ[63:56]
DQS15	Write DQS	DQ[55:52]	DM	N/A
DQS6	Write DQS	DQ[51:48]	Write DQS	DQ[55:48]
DQS14	Write DQS	DQ[47:44]	DM	N/A
DQS5	Write DQS	DQ[43:40]	Write DQS	DQ[47:40]
DQS13	Write DQS	DQ[39:36]	DM	N/A
DQS4	Write DQS	DQ[35:32]	Write DQS	DQ[39:32]
DQS12	Write DQS	DQ[31:28]	DM	N/A
DQS3	Write DQS	DQ[27:24]	Write DQS	DQ[31:24]
DQS11	Write DQS	DQ[23:20]	DM	N/A
DQS2	Write DQS	DQ[19:16]	Write DQS	DQ[23:16]
DQS10	Write DQS	DQ[15:12]	DM	N/A
DQS1	Write DQS	DQ[11:8]	Write DQS	DQ[15:8]
DQS9	Write DQS	DQ[7:4]	DM	N/A
DQS0	Write DQS	DQ[3:0]	Write DQS	DQ[7:0]

## 3.5 Refresh

### 3.5.1 Self-Refresh During Channel Reset

The Advanced Memory Buffer is required to manage DRAM refresh during channel resets and when refresh is enabled through the DAREFTC CSR. When a channel reset event is detected, the Advanced Memory Buffer will take the DRAM's from an unknown state and put them into self-refresh mode. The Advanced Memory Buffer does not track the DRAM state during normal operation, and so has a single process for getting from any DRAM state starting point to the self-refresh state.

When a reset event is detected, the Advanced Memory Buffer's self-refresh FSM will execute the following steps:

1. Clear the DAREFTC.AREFEN CSR to stop the Advanced Memory Buffer auto-refresh engine if enabled.
2. Block all DRAM commands, except those initiated by the self-refresh FSM.
3. Wait until any in-process read or write commands complete, with a minimum wait time of DSREFTC.TCKE, the DRAM "Minimum CKE pulse width time" specification. In-process reads/writes must complete to ensure that the DRAM ODT control outputs are driven low. The minimum time allows for the case where self-refresh entry or power-down entry was executed just before the channel reset.
4. Assert both CKE output pins by setting the DRC.CKE0/1 CSR fields. This will have no effect on the DRAM's if the CKE pins were already asserted.
5. Wait DSREFTC.TXSNR, the DRAM's "Exit self-refresh to a non-read command" specification, to allow any in process DRAM command to complete. This allows time to complete any command that may have been issued just before the channel reset event, such as an auto-refresh, as well as allows for self-refresh exit that may have been initiated when the self-refresh FSM asserted the CKE pins high.
6. Issue a "precharge all" command to both ranks. This guarantees that the DRAM's will be in an "idle" state.
7. Wait as required by DSREFTC.TRP, the DRAM "Precharge time."
8. Issue an auto-refresh command to both ranks. This meets the DRAM requirement that at least one auto-refresh command is issued between any self-refresh exit to self-refresh entry transition.
9. Wait as required by DAREFTC.TRFC, the DRAM "Refresh to active/refresh command time."
10. Issue a self-refresh entry command to both ranks.

When the channel comes out of "fast reset" (exiting the FBD link disable state), the Advanced Memory Buffer will automatically issue a self-refresh exit command to both ranks after the FBD Link Testing State is reached and the Advanced Memory Buffer core clock is stable. Note that this does not apply when the DISSREXIT bit is set as it should be when the Advanced Memory Buffer is powering up, when exiting S3 mode, or when exiting a channel reset that is a part of powering up or exiting S3 mode.

### 3.5.2 Automatic Refresh

The Advanced Memory Buffer has a refresh FSM for issuing auto-refresh commands to the DRAM's on regular intervals. This can be enabled when the DRAM bus is otherwise idle, but not during any other mode that generates DRAM commands, including DRAM power up and initialization, DDR I/O calibration, and normal operation where the FBD channel issues DRAM commands. The DAREFTC CSR controls the refresh interval and period.

### 3.6 Back to Back Turnaround Time

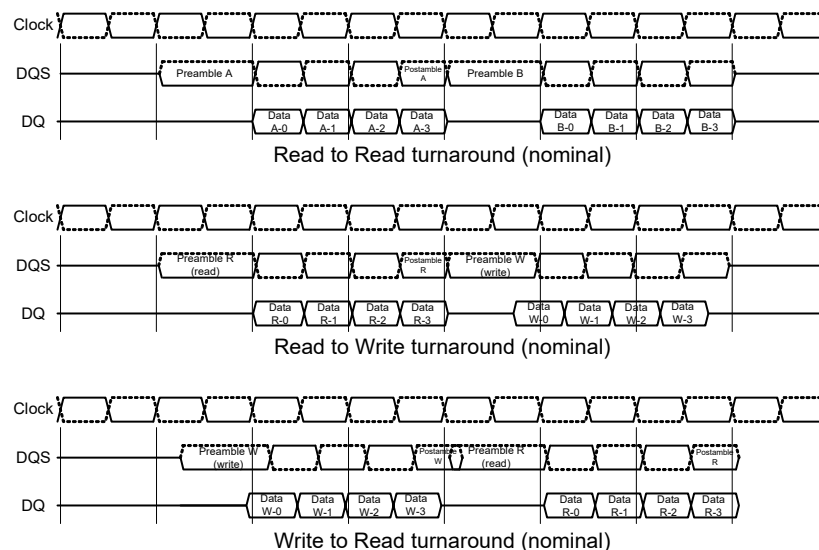
The host controller is required to observe a turnaround time on the DRAM data pins within a DIMM when switching between read and write cycles, and when switching from reads from one rank vs. the other rank on the DIMM. The nominal turnaround time is one clock for each parameter, which is the minimum time required to prevent a collision of the postamble of the first transaction and preamble of the second transaction. Additional clocks may be required by the DIMM, especially at higher speeds.

The three timing parameters are:

- Read to write turnaround time. The number of additional DRAM clocks in which the DRAM data bus must be idle between a read from either rank and a write cycle to either rank.
- Write to read turnaround time. The number of additional DRAM clocks in which the DRAM data bus must be idle between a write to one rank and a read from either rank. The write to read turnaround time to the same rank will generally be dominated by the tWTR specification, which must also be observed.
- Read to read turnaround time. The number of additional DRAM clocks in which the DRAM data bus must be idle between a read from one rank and a read from the opposite rank.

These parameters are dependent on the AMB design and the DIMM PC board layout. The parameters are stored in the SPD. Each parameter is a 2 bit field allowing 0 to 3 additional clocks of turnaround time. See the *SPD Specification* for additional details.

Figure 5 shows the nominal turnaround times, with no additional clocks. Note that the DQS preamble and postamble may merge slightly when the first transaction is at worst case timings and the second transaction is at best case timings.



**Figure 5 — Nominal Turnaround Time Timing Diagram**

### 3.7 DDR Calibration

The following sections describe these DDR calibration and initialization features:

- DRAM initialization and (E)MRS command CSR's and FSM
- DQS failure CSR
- DQS receive enable calibration
- DQS delay calibration

### 3.7 DDR Calibration (cont'd)

#### 3.7.1 DRAM Initialization and (E)MRS

The Advanced Memory Buffer provides a set of CSR's that allow BIOS to manage DRAM power up initialization and set DRAM mode register bits. All commands needed for DRAM initialization can be generated, including precharge, refresh, mode register set (MRS), and extended mode register set EMRS commands. The initialization/ (E)MRS FSM only controls the issuing of single commands, and does not automatically initialize the DRAM. It is the responsibility of software to control the command sequence to correctly initialize the DRAM.

The set of CSR's include the DCALCSR and DCALADDR registers. The fields of these CSR's are described in detail in the configuration register chapter.

The DCALCSR is used to select the command to be issued, which ranks to select, start the FSM that issues the command, and provide completion status.

The DCALADDR sets the bank and address issued to the DRAM, and therefore defines the type of (E)MRS to be issued, including limited OCD commands. DCALADDR[31:16] defines the DDR address bus during these commands, and DCALADDR[2:0] defines the ddr bank address bus.

##### 3.7.1.1 OCD EMRS commands

FB DIMM DRAM timing is set up to work with OCD default calibration. Using the MRS/EMRS registers an EMRS OCD default is sent to the DRAMs. When the DCALCSR bit 31 is cleared to zero, an OCD exit command needs to be sent. When the DCALCSR bit 31 is cleared to zero the DRAMs should be in the default state.

Sending OCD EMRS drive(0), drive(1), adjust or exit OCD cal may have implementation dependent outcomes and should not be used in normal operation.

##### 3.7.1.2 MRS Command Example

The following example shows how to send out an MRS command:

1. Write a value of 0x02320000 to the DCALADDR csr. This will configure the address/bank bus for an MRS command with burst length 4, CAS latency 3, and write recovery 2.
2. Write a value of 0x80000003 to the DCALCSR. This selects the (E)MRS command mode and initiates the FSM that will issue the command.
3. Poll the DCALCSR until bit 31 is cleared to zero by hardware. This indicates that the FSM has completed the selected operation.

#### 3.7.2 Automatic DDR Bus Calibration

The Advanced Memory Buffer has two automatic DDR bus calibration functions that must be executed before read data can be captured reliably. These functions issue a series of write and read transactions on the DRAM bus, analyze the read data captured, and program a set of calibration results configuration registers. During subsequent operations, these configuration registers control the DDR IO circuits and ensure proper data capture. DIMM memory contents are not preserved during calibration. Calibration can take up to several ms to complete. The following steps run the calibration:

1. Program the DCALCSR to 0x8000000c. This selects and initiates the first of two calibrations.
2. Poll the DCALCSR until bit 31 is cleared to zero by hardware.
3. Program the DCALCSR to 0x80000005. This selects/initiates the second calibration.
4. Poll the DCALCSR until bit 31 is cleared to zero by hardware.

### 3.7.3 S3 Recovery Configuration Registers

The following CSRs should be stored in non-volatile memory before entering S3 mode and restored before normal DRAM transactions begin.

- DRC
- MTR
- DSREFTC
- DAREFTC
- S3RESTORE[15:0]
- SPDPAR[15:0] - SPD Personality Bytes

Note: Refer to "Advanced Configuration and Power Interface Specification Version 2.0c" as published by [www.acpi.info](http://www.acpi.info) for S3 mode definition.

### 3.7.4 Receive Enable Calibration

The DQS input receiver needs to be disabled when the DDR bus is floating (tri-stated), e.g., between the read and write data transfers. Otherwise, the floating strobe would cause spurious data to be written into the read data FIFO. Also, the DQS input receiver needs to be disabled during a write so that the write data strobes do not cause unwanted data or check-bits to be written into the read data FIFO.

During a read, the DRAM's initially drive the DQS signals low for a full cycle. This is the preamble. After the preamble, the DQS signals are toggled twice per cycle, for every cycle there is a data transfer, which is determined by the configured burst length and the number of back-to-back read commands that were issued to the selected rank. After the last DQS falling edge, the DQS signal is driven low for a half cycle. This is the post-amble. After the post-amble the DQS signals are tri-stated.

The Advanced Memory Buffer automatically finds the end of the preamble of each of the 18 DQS pairs on the DDR bus. That is, it finds the location of the first waveform transition that defines the end of the preamble of each DQS pair. Once this is complete, the Advanced Memory Buffer calculates the location of the center of the preambles, and stores this information for use during read transactions. Receiver calibration is initiated by setting the DCALCSR.START CSR. Hardware clears this bit when the calibration is complete. The calibration method modifies the data contents of the DIMM.

### 3.7.5 DQS Delay Calibration

The DQS Delay calibration adjusts the Advanced Memory Buffer's on-chip delay circuits that align DQS signals to the center of their associated DQ/CB data eyes at the capture flops in the DDR I/O cluster. This maximizes the DQ/CB setup and hold time at these flops, which capture source synchronous data from the DDR data bus.

DQS delay calibration is initiated by setting the DCALCSR.START CSR. Hardware clears this bit when the calibration is complete. The calibration method modifies the data contents of the DIMM. The calibration is accomplished by issuing a series of write and read transactions, and comparing expected to captured data.

## 3.8 DDR MEMBIST

The AMB supports memory self test for memory initialization during system boot up and for testing the installed memory. During DIMM manufacturing this mode may be used to apply tests at speed to test the AMB-DRAM interface. The table below describes the features of the MEMBIST engine.

At system level MEMBIST may be executed on multiple DIMMs simultaneously. This is expected to speed memory test during system boot.

### 3.8 DDR MEMBIST (cont'd)

During DIMM manufacturing, MEMBIST offers a fast method to detect assembly-related defects, interface defects and the majority of core-related defects during DIMM manufacturing. This testing may be initiated either in or out of band, making MEMBIST compatible with motherboards, low cost ATE, or standalone equipment such as continuity testers. During motherboard testing an FBD-enabled system will be required for in-band.

Transparent mode will be used for memory core testing while BIST will be more useful for DRAM interface testing. For this reason there is no plan to specify a comprehensive BIST capability. Traditional system test methods will be used for operating system or application-based testing of the memory subsystem. This may include existing memory stress tests, applications or other tests selected by the DIMM manufacturer.

#### 3.8.1 MEMBIST Features

##### DATA Type

1. Fixed nibble data patterns (0, 3, 5, 6, 9, A, C, F)
2. 144-bit user defined data pattern and inverted user defined data pattern
3. 32-bit user defined circular shift data pattern
4. Random data generated from LFSR 32-bit CRC data

Those data patterns combined with addressing should be sufficient to test memory interface defect and DIMM assembly-related defect.

##### Address Type

1. Increased or decreased address type controlled by user
2. FastX, FastY, FastXY support
3. User defined test address range

##### DRAM Timing Parameter

1. BL4/BL8 support.
2. Various DDR2 DRAM timing support.
3. DRAM Refresh

##### Failure status:

1. Pass/Fail indicator, test abort, and halt on error features.
2. Up to five failure address recording.
3. Record one, and optionally up to 4, sets of 144 bits failure data.
4. 144 bit failure data location accumulator through entire test.

**3.8.1 MEMBIST Features (cont'd)****Table 3 — MEMBIST Feature Summary**

<b>Failure Status</b>	<b>Pass/Fail indicator</b>
<b>Address Pattern</b>	
X address bits	15-16
Y address bits	15-16
Z address (bank) bits	3
Address pattern in tests	User defined init/end physical address scan with increased/decreased FastX, FastY, FastXY support.
Failure Address logger	Up to 5 failure address loggers.
<b>Data Patterns</b>	
Fixed data pattern	fixed nibble data patterns (0, 3, 5, 6, 9, A, C, F)
User defined data pattern	144 bit data, defined in 5 MBDATA registers by user
LFSR	LFSR (CRC32),
Data Error logger	First 144 bit failure data logger
	144 bits lane failure data location
	Halt on error or run to completion of test
	Test abort during the test
DRAM Timing control	
<b>Programmable Timings</b>	
tCL, tRCD, tRP, tWR, tRC	various DDR2 DRAM timing support
BL	4 or 8
Refresh control	Capable of various DDR2 refresh intervals
<b>BIST Engine</b>	
Access method	all registers and settings could be accessed from FSB or SMBus
DRAM data width	x4 or x8
DRAM initialization and mode register settings	statically set by host
Pattern execution method	SMBus or Host
Failure data access	Failing data is available for read out by the host/SMBus at completion of test
<b>Algorithms Support</b>	
Notation: ^ = increasing addr from start to end v = decreasing addr R/W = Read/Write D/I = Data/ Inverted Data number = sequence of events	



**Table 3 — MEMBIST Feature Summary (Continued)**

Failure Status	Pass/Fail indicator
Scan	$\wedge$ (WD1); $\wedge$ (RD2); $\wedge$ (WI3); $\wedge$ (RI4)
Init	$\wedge$ (WD1)
DATA retention	$\wedge$ (WD1); Pause; $\wedge$ (RD2)
Mats+	$\wedge$ (WD <sub>1</sub> ); $\wedge$ (RD <sub>2</sub> , WI <sub>3</sub> ); $\vee$ (RI <sub>4</sub> , WD <sub>5</sub> );
MarchC–	$\wedge$ (WD1); $\wedge$ (RD2, WI3); $\wedge$ (RI4, WD5); $\vee$ (RD6, WI7); $\vee$ (RI8, WD9); $\vee$ (RD10);
Read	$\wedge$ (RD <sub>1</sub> );

### 3.9 DIMM Organization

The Advanced Memory Buffer supports DIMMs with 1 or 2 independent ranks (chip-selects). Each rank consists of 18 4bit DDR SDRAM devices or 9 8bit DDR SDRAM devices. Dual rank DIMMs consist of 36 4bit DDR SDRAM devices or 18 8bit DDR SDRAM devices. Non-ECC DIMMs could also be built with 16bit DDR SDRAM devices .

## 4 Electrical, Power, and Thermal

This chapter contains a description of the Advanced Memory Buffer's (AMB) electrical DC parameters, timing parameters, power considerations, and thermal considerations.

### 4.1 Electrical DC Parameters

#### 4.1.1 Absolute maximum ratings

Table 4 contains absolute maximum ratings over operating free-air temperature range (see Note 1).

**Table 4 — Absolute Maximum Ratings over Operating Free-air Temperature Range (see NOTE 1)**

Symbol	Parameter	Min	Max	Unit
$V_{DD}$	Supply voltage DRAM Interface	-0.5	+2.3	V
$V_{IN}$ (DDR2), $V_{OUT}$ (DDR2)	Voltage on any DDR2 interface pin relative to $V_{SS}$ (See NOTES 2 and 3)	-0.5	+2.3	V
$I_{INK}$ ( $V_{IN} < 0$ or $V_{IN} > V_{DD}$ )	Input clamp current		$\pm 30$	mA
$I_{OUTK}$ ( $V_{OUT} < 0$ or $V_{OUT} > V_{DD}$ )	Output clamp current		$\pm 30$	mA
$I_{OUT}$ ( $V_{OUT} =$ 0 to $V_{DD}$ )	Continuous output current		$\pm 30$	mA
N/A	Continuous current through each $V_{DD}$ or GND		$\pm 100$	mA
$V_{CC}$	Supply voltage for Core and High Speed Interface	-0.3	+1.75	V
$T_{stg}$	Storage temperature range	-55	+100	°C
NOTE 1	Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.			
NOTE 2	The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.			
NOTE 3	This value is limited to 2.3V maximum.			

#### 4.1.2 Normal Mode

Table 5 contains the electrical DC parameters for the Advanced Memory Buffer part in normal mode.

**Table 5 — Advanced Memory Buffer Normal Mode DC Electrical Parameters**

Parameter		Units	Min	Typ	Max
V <sub>CC</sub> link / core	0 kHz - 30 kHz	Volts	1.455	1.5	1.575
V <sub>DD</sub>		Volts	1.7	1.8	1.9
V <sub>DDSPD</sub>		Volts	3.0	3.3	3.6
NOTE There will also be a V <sub>TT</sub> termination supply at V <sub>DD</sub> /2 available on the DIMM but does not connect to the Advanced Memory Buffer.					

Table 5A contains the electrical DC+AC parameters for the Advanced Memory Buffer part in normal mode.

**Table 5A — Advanced Memory Buffer Normal Mode DC+AC Electrical Parameters**

Parameter		Units	Min	Typ	Max
V <sub>CC</sub> link / core	30 kHz - 1 MHz	Volts	1.425	1.5	1.590
NOTE 1 There is also a +/-5% tolerance allowed for current load steps associated with initialization/error-recovery state transitions, such as into and out of EI, IBIST, and MEMBIST. For these transitions, a temporary voltage overshoot is expected and acceptable as long as it is within +7% (step transition for 20μs and max duty cycle of 10 <sup>-6</sup> ). Transitions between Active and Idle states are not included in this +7%/-5% tolerance.					

Table 6 contains the AMB Power Specification Parameters for the Advanced Memory Buffer part in normal mode.

**Table 6 — AMB Power Specification Parameters and Test Conditions**

Symbol	Conditions	Power Supply	Max	Units	Notes
Idd_Idle_0	<b>Idle Current, single or last DIMM</b> L0 state, idle (0 BW) Primary channel enabled, Secondary Channel Disabled CKE high. Command and address lines stable. DRAM clock active.	@1.5V		mA	
		@1.8V		mA	
		@3.3V		mA	
	<b>Idd_Idle_0 Total Power</b>			W	
Idd_Idle_1	<b>Idle Current, first DIMM</b> L0 state, idle (0 BW) Primary and Secondary channels enabled CKE high. Command and address lines stable. DRAM clock active.	@1.5V		mA	
		@1.8V		mA	
		@3.3V		mA	
	<b>Idd_Idle_1 Total Power</b>			W	
Idd_Idle_2	<b>Idle Current, DRAM power down</b> L0 state, idle (0 BW) Primary and Secondary channels enabled CKE low. Command and address lines floated. DRAM clock active, ODT and CKE driven low.	@1.5V		mA	
		@1.8V		mA	
		@3.3V		mA	

**Table 6 — AMB Power Specification Parameters and Test Conditions (Continued)**

Symbol	Conditions	Power Supply	Max	Units	Notes
Idd_Idle_2 Total Power				W	
Idd_Active_1	Active Power L0 state. 50% DRAM BW, 67% read, 33% write. Primary and Secondary channels enabled. DRAM clock active, CKE high.	@1.5V		mA	
		@1.8V		mA	
		@3.3V		mA	
Idd_Active_1 Total Power				W	
Idd_Active_2	Active Power, data pass through L0 state. 50% DRAM BW to downstream DIMM, 67% read, 33% write. Primary and Secondary channels enabled CKE high. Command and address lines stable. DRAM clock active.	@1.5V		mA	
		@1.8V		mA	
		@3.3V		mA	
Idd_Active_2 Total Power				W	
Idd_L0s	Channel Standby Average power over 42 frames where the channel enters and exits L0s. DRAMs Idle (0 BW). CKE low. Command and address lines floated DRAM clock active, ODE and CKE driven low.	@1.5V		mA	
		@1.8V		mA	
		@3.3V		mA	
Idd_L0s Total Power				W	
Idd_Training (for AMB spec, Not in SPD)	Training Primary and Secondary channels enabled. 100% toggle on all channel lanes DRAMs idle. 0 BW. CKE high, Command and address lines stable. DRAM clock active.	@1.5V		mA	
		@1.8V		mA	
		@3.3V		mA	
Idd_Training Total Power				W	

**Assumptions for all parameters:**

Primary channel Drive strength at 100% with De-emphasis at -6.5dB

Secondary channel drive strength at 60% with De-emphasis at -3dB when enabled.

Address and Data fields are pseudo-random, which provides a 50% toggle rate on DRAM data lines and link lanes when data is being transferred.

Assuming 1 activate command and 1 read/write command per BL=4 transfer

BL=4.

10 lanes southbound and 14 lanes northbound are enabled and active (12 lanes NB if non-ECC DIMM).

**SPD specific assumption:**

Number of devices on the specific DIMM assumed.

Termination of command, address, and control is actual value used on the DIMM.

ECC or non-ECC as per the specific DIMM.

SPD specifies Delta T

#### 4.1.2 Normal Mode (cont'd)

##### AMB power spec specific assumptions:

Dual rank x8 ECC DIMM assumed (18 DRAM devices present on DIMM)

ECC DIMM assumed (72 bit data, 14 lanes northbound).

AMB specification specifies current for each rail.

Table 6A contains the AMB Power Specification Parameters for the Advanced Memory Buffer part in normal mode.

**Table 6A — Table 6 Values for x8 DIMMs**

			533 MHz		667 MHz		800 MHz			
Symbol	Conditions	Power Supply	Thermal Design	Max Current	Thermal Design	Max Current	Thermal Design	Max Current	Units	Notes
Idd_Idle_0	<b>Idle Current, single or last DIMM</b> L0 state, idle (0 BW) Primary channel enabled, Secondary Channel Disabled CKE high. Command and address lines stable. DRAM clock active.	@1.5V	2.1	2.2	2.4	2.6	TBD	TBD	A	
		@1.8V	0.6	0.7	0.6	0.7	TBD	TBD	A	
		@3.3V							A	
Idd_Idle_0 Total Power			3.5		4.0		TBD		W	
Idd_Idle_1	<b>Idle Current, first DIMM</b> L0 state, idle (0 BW) Primary and Secondary channels enabled CKE high. Command and address lines stable. DRAM clock active.	@1.5V	2.7	3.0	3.1	3.4	TBD	TBD	A	
		@1.8V	0.6	0.7	0.6	0.7	TBD	TBD	A	
		@3.3V							A	
Idd_Idle_1 Total Power			4.6		5.1		TBD		W	
Idd_TDP_0  (for AMB spec, Not in SPD)	<b>Active Power, TDP BW, Single or Last DIMM</b> L0 state TDP Channel BW = 2.0GB/s@533; 2.4GB/s@667; 3.0GB/s@800 DIMM BW = 2.0GB/s@533; 2.4GB/s@667; 3.0GB/s@800 67% read, 33% write. Primary channel Enabled Secondary channel Disabled CKE high. Command and Address	@1.5V	2.4	2.6	2.8	3.0	TBD	TBD	A	1
		@1.8V	1.1	1.3	1.2	1.3	TBD	TBD	A	1
		@3.3V							A	
Idd_TDP_0 Total Power			5.2		5.8		TBD		W	1
Idd_TDP_1  (for AMB spec, Not in SPD)	<b>Active Power, TDP BW, First DIMM</b> L0 state TDP Channel BW = 2.0GB/s@533; 2.4GB/s@667; 3.0GB/s@800 DIMM BW =2/3 Channel BW = 1.3GB/s@533; 1.6GB/s@667; 2GB/s@800 67% read, 33% write. Primary channel Enabled Secondary channel Enabled CKE high. Command and Ad	@1.5V	3.0	3.3	3.5	3.8	TBD	TBD	A	1
		@1.8V	0.9	1.0	0.9	1.0	TBD	TBD	A	1
		@3.3V							A	
Idd_TDP_1 Total Power			5.8		6.4		TBD		W	1

**Table 6A — Table 6 Values for x8 DIMMs (Continued)**

			533 MHz		667 MHz		800 MHz			
Symbol	Conditions	Power Supply	Thermal Design	Max Current	Thermal Design	Max Current	Thermal Design	Max Current	Units	Notes
Idd_Active_1	<b>Active Power</b> L0 state. 50% DRAM BW, 67% read, 33% write. Primary and Secondary channels enabled. DRAM clock active, CKE high.	@1.5V	3.1	3.4	3.6	3.9	TBD	TBD	A	
		@1.8V	1.2	1.3	1.2	1.3	TBD	TBD	A	
		@3.3V							A	
Idd_Active_1 Total Power			6.4		7.1		TBD		W	
Idd_Active_2	<b>Active Power, data pass through</b> L0 state. 50% DRAM BW to downstream DIMM, 67% read, 33% write. Primary and Secondary channels enabled CKE high. Command and address lines stable. DRAM clock active.	@1.5V	2.9	3.2	3.3	3.7	TBD	TBD	A	
		@1.8V	0.6	0.7	0.6	0.7	TBD	TBD	A	
		@3.3V							A	
Idd_Active_2 Total Power			5.0		5.6		TBD		W	
Idd_Training (for AMB spec, Not in SPD)	<b>Training</b> Primary and Secondary channels enabled. 100% toggle on all channel lanes DRAMs idle. 0 BW. CKE high, Command and address lines stable. DRAM clock active.	@1.5V		3.5		4.0	TBD	TBD	A	
		@1.8V		0.7		0.7	TBD	TBD	A	
		@3.3V							A	
Idd_Training Total Power							TBD		W	
Idd_IBIST (for AMB spec, Not in SPD)	<b>IBIST</b> Over all IBIST modes DRAM Idle (0 BW) Primary channel Enabled Secondary channel Enabled CKE high. Command and Address lines stable DRAM clock active	@1.5V		3.8		4.5	TBD	TBD	A	
		@1.8V		0.7		0.7	TBD	TBD	A	
		@3.3V							A	
Idd_IBIST Total Power							TBD		W	
Idd_MemBIST (for AMB spec, Not in SPD)	<b>MemBIST</b> Over all MemBIST modes >50% DRAM BW (as dictated by the AMB) Primary channel Enabled Secondary channel Enabled CKE high. Command and Address lines stable DRAM clock active	@1.5V		3.3		3.8	TBD	TBD	A	
		@1.8V		2.1		2.1	TBD	TBD	A	
		@3.3V							A	
Idd_MemBIST Total Power							TBD		W	
Idd_EI (for AMB spec, Not in SPD)	<b>Electrical Idle</b> DRAM Idle (0 BW) Primary channel Disabled Secondary channel Disabled CKE low. Command and Address lines Floated DRAM clock active, ODT and CKE driven low	@1.5V		2.0		2.5	TBD	TBD	A	
		@1.8V		0.2		0.2	TBD	TBD	A	
		@3.3V							A	
Idd_EI Total Power							TBD		W	

### 4.1.2 Normal Mode (cont'd)

Table 6B contains the AMB Power Specification Parameters for the Advanced Memory Buffer part in normal mode.

**Table 6B — Table 6 Values for x4 DIMMs**

			533 MHz		667 MHz		800 MHz			
Symbol	Conditions	Power Supply	Thermal Design	Max Current	Thermal Design	Max Current	Thermal Design	Max Current	Units	Notes
Idd_Idle_0	<b>Idle Current, single or last DIMM</b> L0 state, idle (0 BW) Primary channel enabled, Secondary Channel Disabled CKE high. Command and address lines stable. DRAM clock active.	@1.5V	2.1	2.2	2.4	2.6	TBD	TBD	A	
		@1.8V	0.9	0.9	0.9	0.9	TBD	TBD	A	
		@3.3V							A	
Idd_Idle_0 Total Power			3.9		4.4		TBD		W	
Idd_Idle_1	<b>Idle Current, first DIMM</b> L0 state, idle (0 BW) Primary and Secondary channels enabled CKE high. Command and address lines stable. DRAM clock active.	@1.5V	2.7	3.0	3.1	3.4	TBD	TBD	A	
		@1.8V	0.9	0.9	0.9	0.9	TBD	TBD	A	
		@3.3V							A	
Idd_Idle_1 Total Power			4.9		5.5		TBD		W	
Idd_TDP_0  (for AMB spec, Not in SPD)	<b>Active Power, TDP BW, Single or Last DIMM</b> L0 state TDP Channel BW = 2.0GB/s@533; 2.4GB/s@667; 3.0GB/s@800 DIMM BW = 2.0GB/s@533; 2.4GB/s@667; 3.0GB/s@800 67% read, 33% write. Primary channel Enabled Secondary channel Disabled CKE high. Command and Address	@1.5V	2.4	2.6	2.8	3.0	TBD	TBD	A	1
		@1.8V	1.5	1.6	1.5	1.6	TBD	TBD	A	1
		@3.3V							A	
Idd_TDP_0 Total Power			5.9		6.5		TBD		W	1
Idd_TDP_1  (for AMB spec, Not in SPD)	<b>Active Power, TDP BW, First DIMM</b> L0 state TDP Channel BW = 2.0GB/s@533; 2.4GB/s@667; 3.0GB/s@800 DIMM BW =2/3 Channel BW = 1.3GB/s@533; 1.6GB/s@667; 2GB/s@800 67% read, 33% write. Primary channel Enabled Secondary channel Enabled CKE high. Command and Ad	@1.5V	3.0	3.3	3.5	3.8	TBD	TBD	A	1
		@1.8V	1.3	1.4	1.3	1.4	TBD	TBD	A	1
		@3.3V							A	
Idd_TDP_1 Total Power			6.3		6.9		TBD		W	1
Idd_Active_1	<b>Active Power</b> L0 state. 50% DRAM BW, 67% read, 33% write. Primary and Secondary channels enabled. DRAM clock active, CKE high.	@1.5V	3.1	3.4	3.6	3.9	TBD	TBD	A	
		@1.8V	1.6	1.7	1.6	1.7	TBD	TBD	A	
		@3.3V							A	
Idd_Active_1 Total Power			6.9		7.6		TBD		W	

### Table 6B — Table 6 Values for x4 DIMMs (Continued)

			533 MHz		667 MHz		800 MHz			
Symbol	Conditions	Power Supply	Thermal Design	Max Current	Thermal Design	Max Current	Thermal Design	Max Current	Units	Notes
Idd_Active_2	Active Power, data pass through L0 state. 50% DRAM BW to downstream DIMM, 67% read, 33% write. Primary and Secondary channels enabled CKE high. Command and address lines stable. DRAM clock active.	@1.5V	2.9	3.2	3.3	3.7	TBD	TBD	A	
		@1.8V	0.9	0.9	0.9	0.9	TBD	TBD	A	
		@3.3V							A	
Idd_Active_2 Total Power			5.5		6.1		TBD		W	
Idd_Training (for AMB spec, Not in SPD)	Training Primary and Secondary channels enabled. 100% toggle on all channel lanes DRAMs idle. 0 BW. CKE high, Command and address lines stable. DRAM clock active.	@1.5V		3.5		4.0	TBD	TBD	A	
		@1.8V		0.9		0.9	TBD	TBD	A	
		@3.3V							A	
Idd_Training Total Power							TBD		W	
Idd_IBIST (for AMB spec, Not in SPD)	IBIST Over all IBIST modes DRAM Idle (0 BW) Primary channel Enabled Secondary channel Enabled CKE high. Command and Address lines stable DRAM clock active	@1.5V		3.8		4.5	TBD	TBD	A	
		@1.8V		0.9		0.9	TBD	TBD	A	
		@3.3V							A	
Idd_IBIST Total Power							TBD		W	
Idd_MemBIST (for AMB spec, Not in SPD)	MemBIST Over all MemBIST modes >50% DRAM BW (as dictated by the AMB) Primary channel Enabled Secondary channel Enabled CKE high. Command and Address lines stable DRAM clock active	@1.5V		3.3		3.8	TBD	TBD	A	
		@1.8V		2.4		2.4	TBD	TBD	A	
		@3.3V							A	
Idd_MemBIST Total Power							TBD		W	
Idd_EI (for AMB spec, Not in SPD)	Electrical Idle DRAM Idle (0 BW) Primary channel Disabled Secondary channel Disabled CKE low. Command and Address lines Floated DRAM clock active, ODT and CKE driven low	@1.5V		2.0		2.5	TBD	TBD	A	
		@1.8V		0.2		0.2	TBD	TBD	A	
		@3.3V							A	
Idd_EI Total Power							TBD		W	
NOTE 1 Values highlighted in ‘Red’ are for reference (i.e., placeholder value)										



#### 4.1.2 Normal Mode (cont'd)

##### Notes and Assumptions:

V<sub>dd</sub> : Thermal Design = 1.845V (+2.5%) ; Max Current = 1.900V (+5.5%)

V<sub>cc</sub> : Thermal Design = 1.530V (+2%) ; Max Current = 1.575V (+5%)

Includes all DIMM DRAM organizations (SRx4, DRx4, SRx8, DRx8) and Raw Cards (A, B, C, D, E, H, J)

For x8, measured with DRx8 raw card B with 39 ohm termination for command, address, and clocks, and 47 ohm termination for CS and CKE

For x4, measured with DRx4 raw card E with parallel 33 ohm termination for command, address, and 39 ohm termination for CS, CKE and clocks

Note: cards using smaller termination resistors will have higher powers. e.g., x4 cards parallel 22 ohm termination for command and address could add as much as 0.4W to the power for all states.

Primary channel Drive strengths at 100% with De-emphasis at -6.5dB

Secondary channel Drive strengths at 60% with De-emphasis at -3.5dB when enabled

Address and Data fields are pseudo-random, which provides a 50% toggle rate on DRAM data lines and link lanes when data is being transferred.

Assuming 1 activate command and 1 read/write command per BL=4 transfer BL=4.

10 lanes southbound and 14 lanes northbound are enabled and active (12 lanes NB if non-ECC DIMM).

V<sub>ddspd</sub> rail assumed to be insignificant (<0.1 A max @ 3.3v)

Thermal Max is for cooling and heat sink / heat spreader requirements

VR Max is for voltage regulator sizing and voltage distribution and tolerance requirements

Total Power assumes some 1.8v current is dissipated in the DIMM terminations (not in the AMB)

S3 is an ACPI mode in which the DIMMs are put into a very lower power state, with the DRAMs in self refresh mode. This AMB S3 current specification is required for the sizing of the power supply used for the S3 mode.

DRAMs in self refresh.

REFCLK not toggling.

$$VDD = VDD_{max} (1.9V).$$
$$V_{CC} = 0V$$
$$V_{TT} = 0V$$

			533 MHz		667 MHz		800 MHz		
Symbol	Conditions	Power Supply	Nominal	Max Current	Nominal	Max Current	Nominal	Max Current	Units
Idd_S3	<b>S3 current</b> VDD = 1.9V VCC = 0V VTT = 0V Across process variations Across the operating TCASE temperature range. DIMM types: Raw Card A, B, C, D, E, H, J, and future raw card type as adopted by FR-DIMM	VDD (1.8V)		75		75		75	mA

Note that the total DIMM current will include the AMB IDD\_S3 value as well as the self refresh current of all of the DRAMs on the DIMM.

Refer to “High Speed Differential PTP Link at 1.5V Specification” for recommended operating conditions.

Table 7 contains the FBD electrical timing specifications.

[illegible]

Parameter	Date Rate	Min	Typ	Max	Units	Comments
tSCL Southbound Command Latency	533				ns	1, 8, 9
	667				ns	
	800				ns	
tNDL Northbound Data Latency	533				ns	2, 9
	667				ns	
	800				ns	
tCCL Core Command Latency	533				ns	3, 5
	667				ns	
	800				ns	
tCDL Core Data Latency	533				ns	4, 5
	667				ns	
	800				ns	
tRESAMPLE Resample Delay	533				ns	6
	667				ns	
	800				ns	
tRESYNC Resync Delay	533				ns	7, 8, 9
	667				ns	
	800				ns	

NOTE 1 tSCL is measured from the center of the data eye of the first bit of the command frame at the SB input to the DDR clock rising edge that latches the A-slot command to the DRAMs. See diagram below.

NOTE 2 tNDL is measured from the rising edge of the latest DQS input to the AMB to the center of the data eye of the first bit of the matching data frame at the NB outputs. See diagram below.

NOTE 3 tCCL is calculated as the maximum time from an internal point where the deskewed frame aligned command is available to the core from the SB IO (the start of the Command to Data Delay) until the DDR clock rising edge that latches the A-slot command to the DRAMs. See diagram below. This maximum considers worst case operating conditions.

NOTE 4 tCDL is calculated as the maximum time from the rising edge of the latest DQS input to the time where the data is available to be sent to the NB IO (end point of the Command to Data Delay). See diagram below. This maximum considers worst case operating conditions.

NOTE 5 tCCL and tCDL are meant to provide the DIMM vendor with the AMB portion of the Command to Data delay which is included in the SPD. The Command to Data Delay in the SPD consists of tCCL + tCMD\_FLT + tDQSCK (DRAM spec) + tDQS\_FLT + tCDL. The XXXX\_FLT parameters are PCB flight delays. tSCL may have a programmable added delay on some DIMM configurations which must also be added in.

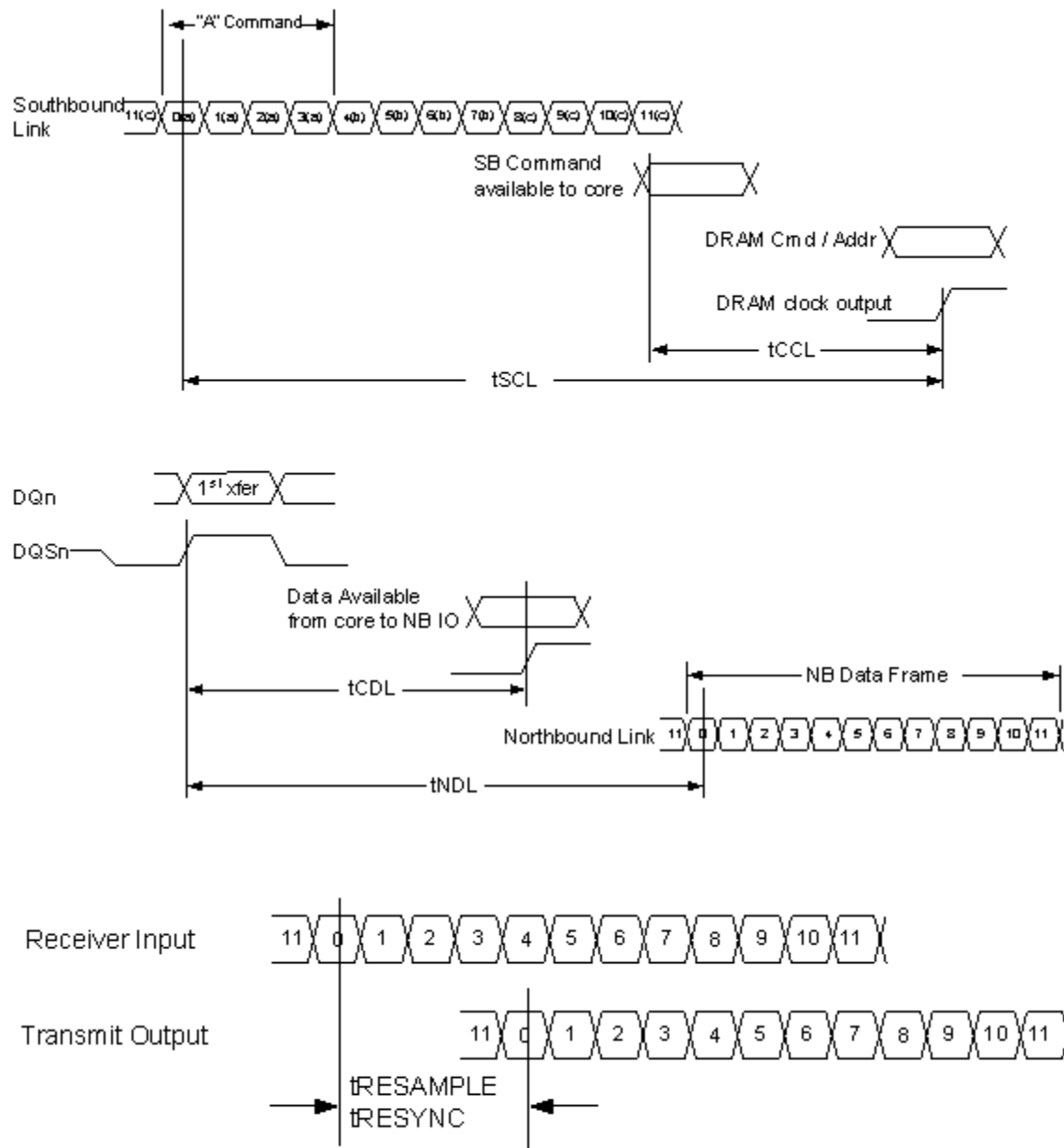
NOTE 6 tRESAMPLE is the delay from the southbound input to the southbound output, or the northbound input to the northbound output when in resample mode, measured from the center of the data eye.

NOTE 7 tRESYNC is the delay from the southbound input to the southbound output, or the northbound input to the northbound output when in resync mode, measured from the center of the data eye.

NOTE 8 Measured upon entering L0 state immediately after channel reset, before the input has drifted with respect to REFCLK.

NOTE 9 Typical numbers include the average of any clock synchronizing.

## 4.2.2 AMB Latency Parameters (cont'd)



#### 4.2.2.1 AMB Latency Range

Description	Parameter	Data Rate	Min	Max	Units	Comments
<b>Command to Data Latency</b>	tC2D_AMB	533	20.3	25.1	ns	1
		667	17.1	21.1	ns	
		800	TBD	TBD	ns	
<b>Southbound Command Latency</b>	tSCL	533			ns	2
		667			ns	
		800			ns	
<b>Northbound Data Latency</b>	tNDL	533			ns	2
		667			ns	
		800			ns	
<b>Core Command Latency</b>	tCCL	533			ns	2
		667			ns	
		800			ns	
<b>Core Data Latency</b>	tCDL	533			ns	2
		667			ns	
		800			ns	
<b>RESAMPLE Delay</b>	tRESAMPLE_AMB_SB	533	0.9	2.2	ns	3
	tRESAMPLE_AMB_NB	533	0.9	2.2	ns	4
	tRESAMPLE_AMB_SB	667	0.9	1.9	ns	3
	tRESAMPLE_AMB_NB	667	0.9	1.9	ns	4
	tRESAMPLE_AMB_SB	800	TBD	TBD	ns	3
	tRESAMPLE_AMB_NB	800	TBD	TBD	ns	4
<b>RESYNC Delay</b>	tRESYNC_AMB_SB	533	2.3	3.9	ns	5
	tRESYNC_AMB_NB	533	2.3	3.9	ns	6
	tRESYNC_AMB_SB	667	2.0	3.2	ns	5
	tRESYNC_AMB_NB	667	2.0	3.2	ns	6
	tRESYNC_AMB_SB	800	TBD	TBD	ns	5
	tRESYNC_AMB_NB	800	TBD	TBD	ns	6
<p>NOTE 1 <b>tC2D_AMB</b> = Measured delay at AMB balls between the center of the 1st UI of command frame on the primary southbound lane 8<sup>1</sup> (AMB balls U29 and U28) and the center of the 1st UI of return data on the primary northbound lane 0 (AMB balls U1 and U2) - CL (DRAM CAS latency) value * frame clock period - AL (DRAM additional latency) value * frame clock period.</p> <p>NOTE 2 These parameters are included in the Command to Data Latency tC2D_AMB and there is no need for them to be specified individually for interoperability.</p> <p>NOTE 3 <b>tRESAMPLE_AMB_SB</b> = Measured delay at AMB balls between the center of the 1st UI of a frame on the primary southbound lane 8 (AMB balls U29 and U28) and the center of the 1st UI of the same frame on the secondary southbound lane 8 (AMB balls Y26 and W26).</p> <p>NOTE 4 <b>tRESAMPLE_AMB_NB</b> = Measured delay at AMB balls between the center of the 1st UI of a frame on the secondary northbound lane 0 (AMB balls V4 &amp; V5) and the center of the 1st UI of the same frame on the primary northbound lane 0 (AMB balls U1 and U2).</p> <p>NOTE 5 <b>tRESYNC_AMB_SB</b> = Measured delay at AMB balls between the center of the 1st UI of a frame on the primary southbound lane 8 (AMB balls U29 and U28) and the center of the 1st UI of the same frame on the secondary southbound lane 8 (AMB balls Y26 and W26)..</p> <p>NOTE 6 <b>tRESYNC_AMB_NB</b> = Measured delay at AMB balls between the center of the 1st UI of a frame on the secondary northbound lane 0 (AMB balls V4 and V5) and the center of the 1st UI of the same frame on the primary northbound lane 0 (AMB balls U1 and U2).</p>						

<sup>1</sup> This definition assumes that SB lane 8 is the latest lane to arrive at the AMB balls. This will typically be the case since SB lane 8 is the longest SB lane on FBDIMMs. If, due to large lane-to-lane skew at the DIMM gold finger, another lane is the latest lane to arrive at the AMB balls this other lane must be used instead for the tC2D\_AMB measurement.

#### 4.2.2.2 AMB CMD2DATANXT Utilization for Merge Data Training

AMB designs support a limited range of CMD2DATANXT register (refer to 11.3.4.1 in Register chapter) settings during runtime.

The AMB CMD2DATANXT mechanism will be used temporarily by firmware during memory subsystem training to ensure each memory channel with adequate timing margin to prevent Merge Data Errors when mixing different AMB's on a channel. Firmware will over ride the SPD CMD2DATANXT value only during TS2<sup>2</sup>, and not while accessing DRAM. Firmware can set the Next Value of Command to Data Delay by as much as 16UI higher than what is programmed in the SPD. The new value will be used after the next fast reset. Once training is completed, the original CMD2DATANXT value from the SPD will be restored. The original value of the Command to Data Delay will take effect after the next fast reset before normal system operation initiates.

AMB designs need to support a range of CMD2DATANXT values for purposes of non-DRAM access, Merge Data training ONLY. The supported range needs to extend at least 16UI higher than the value programmed in the SPD for normal operation.

AMB designs that do not support a particular DLYFRAC value due implementation granularity must functionally round up to the next supported value.

<sup>2</sup> **TS2** – Used during the Polling state to determine the round trip latency of the channel and to test that each individual AMB can perform data merge properly.

### 4.3 DDR2 DRAM Interface Electrical Specifications

Table 8 contains the electrical DC parameters for the DDR2 DRAM Interface on an AMB.

**Table 8 — Recommended Operating Conditions for DRAM Interface**

Symbol	Parameter	Min	Nom	Max	Unit
$V_{DD}$	Supply voltage	1.7	1.8	1.9	V
$V_{REF}$	Input reference voltage	$0.49 * V_{DD}$	$0.50 * V_{DD}$	$0.51 * V_{DD}$	mV
$V_{TT}$	Termination voltage	$V_{REF} - 40$	$V_{REF}$	$V_{REF} + 40$	mV
<b>Single Ended Signals</b>					
$V_{IN}$	Input voltage	0	-	$V_{DD}$	
$V_{IH(dc)}$	DC HIGH-level input voltage	$V_{DD} / 2 + 100$	-	$V_{DD} + 300$	mV
$V_{IL(dc)}$	DC LOW-level input voltage	-300	-	$V_{DD} / 2 - 100$	mV
$V_{IH(ac)}$	AC HIGH-level input voltage	$V_{DD} / 2 + 200$	-	-	mV
$V_{IL(ac)}$	AC LOW-level input voltage	-	-	$V_{DD} / 2 - 200$	mV
$V_{OH}$	Minimum Required Output Pull-up under AC Test Load	$V_{DD} / 2 + 400$	-	-	mV
$V_{OL}$	Maximum Required Output Pull-down under AC Test Load	-	-	$V_{DD} / 2 - 400$	mV
$V_{OTR}$	Output Timing Measurement Reference Level	-	$0.5 * V_{DD}$	-	V
$I_{OH(dc)}$	Output minimum source dc current	-13.8	-	-	mA
$I_{OL(dc)}$	Output minimum sink dc current	13.8	-	-	mA
<b>Differential Signals</b>					
$V_{ID(dc)}$	DC differential input voltage	0.2	-	-	V
$V_{ID(ac)}$	AC differential input voltage	0.4	-	-	V
$V_{IX(ac)}$	AC differential input crossing voltage	$0.5 * V_{DD} - 0.175$	-	$0.5 * V_{DD} + 0.175$	V
$V_r$	Input timing measurement reference level		$V_{IX(ac)}$		
$V_{OX(ac)}$	AC differential output crossing voltage	$0.5 * V_{DD} - 0.125$	-	$0.5 * V_{DD} + 0.125$	V
$V_{OUT(slew)}$	Output slew-rate requirement	2.2	-	3.2	V/ns
$I_{lh}$	Input leakage current (HIGH)	-	-	10	uA
$I_{ll}$	Input leakage current (LOW)	-	-	10	uA
$C_{IO}$	Input/Output Capacitance	2.0	-	2.5	pF
$R_{OUT}$	Output Impedance	13	-	20	Ohms
$T_C$	Package surface (case) temperature for AMB (In our case, $T_C = T_J$ )	-	-	110	°C

### 4.3 DDR2 DRAM Interface Electrical Specifications (cont'd)

NOTE 1 Values highlighted in 'Red' are for reference (i.e., placeholder value)

NOTE 2 No  $V_{REF}$  pin on AMB

NOTE 3  $V_{OUT(slew)}$  covers all other outputs slew rate including clock

NOTE 4 Input voltage for all pins is limited to a maximum of 2.3v

NOTE 5  $V_{DD}/2 = 1.7/2 = 850\text{mV}$ ;  $V_{OUT} = 575\text{mV}$ .  $(V_{OUT} - V_{DD}/2)/I_{OH}$  must be less than 20 Ohm for values of  $V_{OUT}$  between  $V_{DD}/2$  and  $V_{DD}/2 - 275\text{mV}$ .

NOTE 6  $V_{DD}/2 = 1.7/2 = 850\text{mV}$ ;  $V_{OUT} = 275\text{mV}$ .  $V_{OUT}/I_{OH}$  must be less than 20 Ohm for values of  $V_{OUT}$  between 0V and 275mV.

NOTE 7  $C_{IO}$  is the Input/Output capacitance for DQ/DQS, and Output capacitance for CMD/ADDR/CK

NOTE 8  $V_{OH}/V_{OL}$  values apply to all drivers, except when de-emphasis is used by the drivers

This chapter contains a description of the Advance Memory Buffer component's AC electrical parameters

### 4.4 DDR2 Electrical Output Timing Specifications

#### 4.4.1 Description of DQ/DQS Alignment

The DQS output rising edge aligns with the CLK output rising edge and the DQS output falling edge aligns with the CLK output falling edge. The DQ outputs are 1/4 cycle offset from the DQS outputs.

DQ/DQS inputs are edge aligned and will be skewed by internal receiver DLL. Inputs are terminated on-die by a resistive circuit during reads only.

#### 4.4.2 Description of ADD/CMD/CNTL Outputs

ADD/CMD/CNTL outputs can be adjusted relative to CLK (see Table 9.) to improve setup or hold times. The value of this delay is fixed at boot time. These outputs are either aligned with CLK falling, or with a certain timing offset before CLK falling. The amount of offset is implementation specific (e.g., can be a constant timing offset, or a known ratio of the DRAM clock period).

#### 4.4.3 Test Load Specification

DDR2 timings are specified for a 25 Ohm test load terminated to  $V_{dd}/2$ , measured at the Advance Memory Buffer component package pins.

#### 4.4.4 tDVA and tDVB Parameter Description

The timing parameters tDVA and tDVB indicate the time the DQ is valid after or before DQS. tDVA is used to indicate the time that Data is Valid After. tDVA is used for DQ/DQS write hold calculations (tDH). tDVB is used to indicate the time that Data is Valid Before. tDVB is used for DQ/DQS write setup calculations (tDS).



#### 4.4.4 tDVA and tDVB Parameter Description (cont'd)

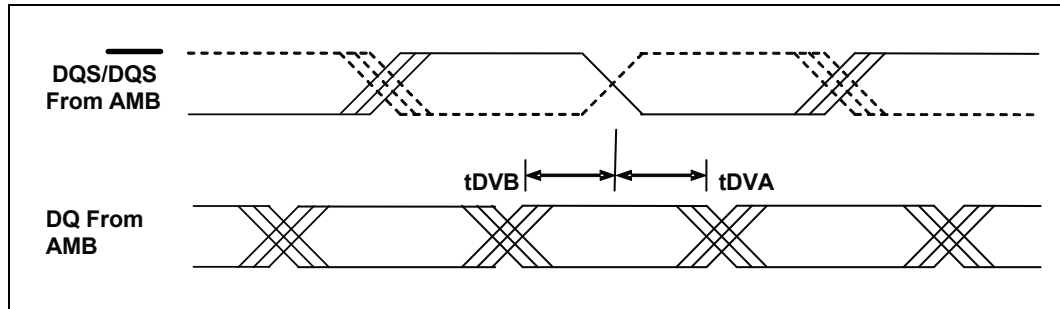


Figure 6 — tDVA and tDVB Timing Diagram

#### 4.4.5 tjit and tjit<sub>HP</sub> Parameter Description

The parameter tjit is the full period jitter, and tjit<sub>HP</sub> is the half-period jitter.

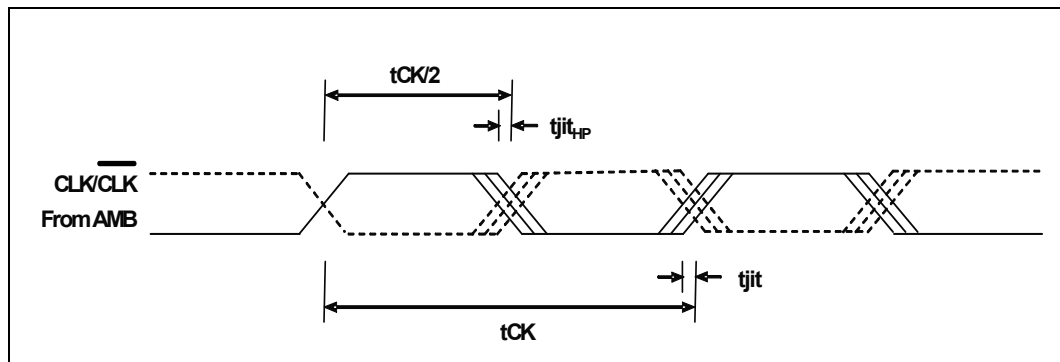


Figure 7 — tjit and tjit<sub>HP</sub> Timing Diagram

#### 4.4.6 tCVA, tCVB, tECVA and tECVB Parameter Description

The parameters tCVA and tCVB specify the time that command is valid after and before CLK. tCVA stands for the time that the Command is Valid After the CLK/CLK crossing point. tCVA is used for CA/CLK hold calculations (tIH). tCVB stands for the time that the Command is Valid Before the CLK/CLK crossing point. tCVB is used for CA/CLK setup calculations (tIS). Figure 8 shows tCVA and tCVB.

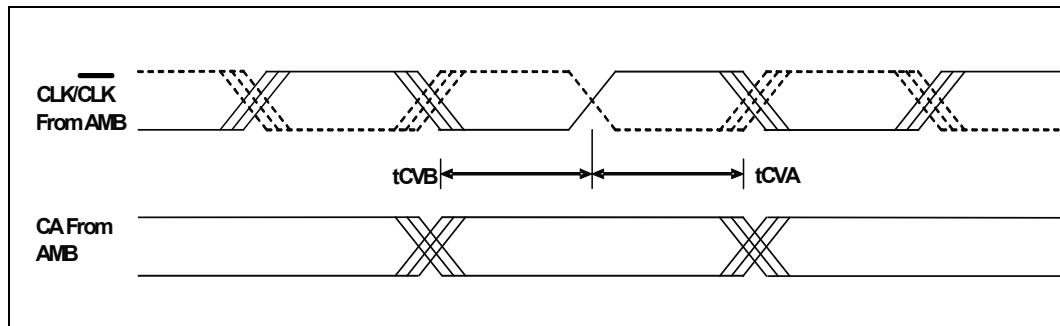


Figure 8 — tCVA and tCVB Timing Diagram

#### 4.4.6 tCVA, tCVB, tECVA and tECVB Parameter Description (cont'd)

tECVA and tECVB apply in early mode. For DIMMs with 36 devices, the command, address and control signals can be shifted by 1/6 clock in early mode. Figure 9 shows tECVA and tECVB.

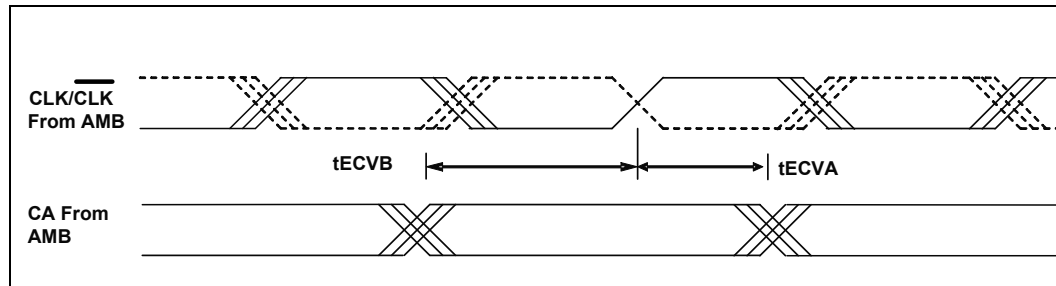


Figure 9 — tECVA and tECVB Timing Diagram

#### 4.4.7 tDQSCK Timing Parameter Description

tDQSCK indicated the CLK to DQS delay. This value is used for tDQSS, tDSS and tDSH timing calculations. In order to determine these numbers accurately, package parameters must be taken into account. This adjusts the minimum time by -110 ps and the maximum by -70 ps.

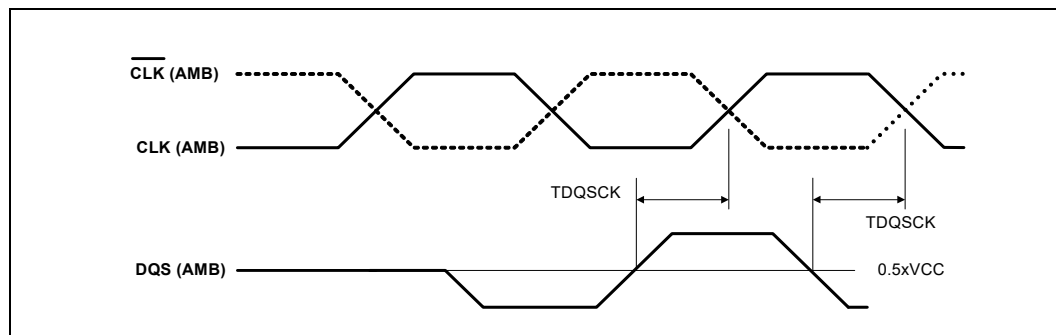


Figure 10 — TDQSCK Timing Diagram

#### 4.4.8 DQ and CB (ECC) Setup/Hold Relationships to/from DQS (Read Operation)

Table shows the timing diagram for tHDamb and tSUamb. The data is launched from the DRAM “edge aligned,” meaning that the DQ data signals switch coincident with the DQS strobe rising and falling edges. Internal to the Advance Memory Buffer, the DQS strobe is delayed by approximately a quarter clock, and this delayed clock is then used to capture the DQ data. Thus, the setup time tSUamb is negative, meaning that the data can arrive at the Advance Memory Buffer inputs after the strobe, and tHDamb is greater than a quarter clock, so that the data will not change until after it has been captured by the internally delayed strobe. The Advance Memory Buffer determines the correct internal delay of strobe DQS based on a search of the data eye during the initialization of the system. The tHDamb and tSUamb specifications are based on an idealized data eye, where the search delays the strobe by exactly one quarter clock. The sum of tHDamb and tSUamb is equivalent to the minimum data valid window at the Advance Memory Buffer inputs.

#### 4.4.8 DQ and CB (ECC) Setup/Hold Relationships to/from DQS (Read Operation) (cont'd)

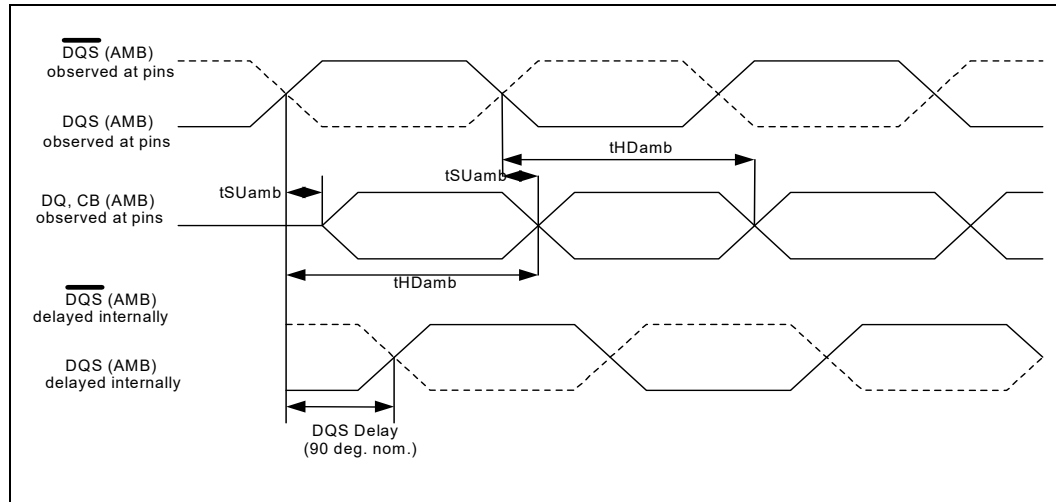


Figure 11 — DQ and CB (ECC) Setup/Hold Relationship to/from DQS Timing Diagram

#### 4.4.9 Write Preamble Duration

The write preamble duration is the measurement from the point when DQS and  $\overline{\text{DQS}}$  start to be driven, to the crossing point of DQS and  $\overline{\text{DQS}}$ . Typically, to determine when DQS and  $\overline{\text{DQS}}$  are starting to be driven, timing measurements are made at  $0.5 \times \text{VCC} \pm 50 \text{ mV}$ , and  $0.5 \times \text{VCC} \pm 100 \text{ mV}$ , and then the measurements are linearly extrapolated back to  $0.5 \times \text{VCC}$ .

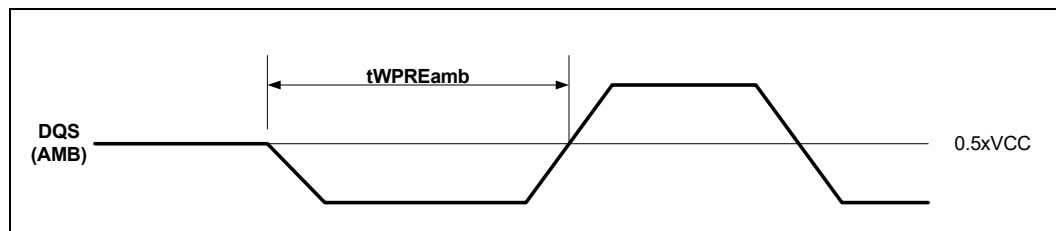


Figure 12 — Write Preamble Duration Timing Diagram

#### 4.4.10 Write Postamble Duration

The write postamble duration is the measurement from the crossing point of DQS and  $\overline{\text{DQS}}$ , to the point where DQS and  $\overline{\text{DQS}}$  start to go into a high impedance state. Typically, to determine when DQS and  $\overline{\text{DQS}}$  are starting to go into a high impedance state, for DQS, timing measurements are made at  $\text{Vlow} + 50 \text{ mV}$ , and  $\text{Vlow} + 100 \text{ mV}$ , and then the measurements are linearly extrapolated back to  $\text{Vlow}$ . For  $\overline{\text{DQS}}$ , timing measurements are made at  $\text{Vhigh} - 50 \text{ mV}$ , and  $\text{Vhigh} - 100 \text{ mV}$ , and then the measurements are extrapolated back to  $\text{Vhigh}$ .

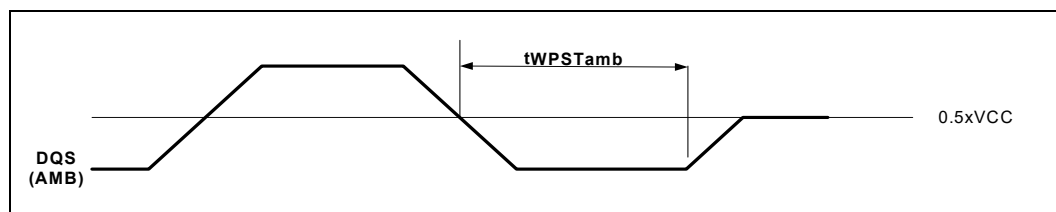


Figure 13 — Write Postamble Duration Timing Diagram

#### 4.4.11 Advance Memory Buffer Component Electrical Timing Summary

Table 9 and Table 6-2 contain the electrical timing specifications for the Advance Memory Buffer component DDR2 interface.

**Table 9 — Advance Memory Buffer Component DDR2 Electrical Timing Specifications  
(Sheet 1 of 2)**

**Note: Values in the DDR2 800 column are for example only. Subject to change based on JEDEC DDR2 Specification timing closure).**

Symbol	Parameter	DDR2 800		DDR2 667		DDR2 533		Units	Fig #
		Min	Max	Min	Max	Min	Max		
System Memory Clock Timings									
t <sub>CK</sub>	Ideal clock (CK) period	2.5		3.0		3.75		ns	
t <sub>CH</sub>	CK high time	1.12		1.35		1.70		ns	
t <sub>CL</sub>	CK low time	1.12		1.35		1.70		ns	
t <sub>jit</sub>	CK cycle to cycle Jitter		130		150		175	ps	4-7
t <sub>jit</sub> <sub>HP</sub>	CK half-cycle jitter		130		150		175	ps	4-7
TDQSCK	Clock rising edge to DQS rising edge, or clock falling edge to DQS falling edge - includes -110/-70 ps for package	-190	10	-200	20	-210	30	ps	4-10
System Memory Address/Command/Control Signal Timings (Normal)									
t <sub>CVB</sub>	CMD/ADD/CNTL output valid before CLK/ <u>CLK</u>	1030		1260		1615		ps	4-8
t <sub>CVA</sub>	CMD/ADD/CNTL output valid after CLK/ <u>CLK</u> - includes -140 ps for package	890		1120		1475		ps	4-8
System Memory Address/Command/Control Signal Timings (Early)									
t <sub>ECVB</sub>	Early CMD/ADD/CNTL output valid before CLK/ <u>CLK</u>	1440		1760		2240			4-9
t <sub>ECVA</sub>	Early CMD/ADD/CNTL output valid after CLK/ <u>CLK</u> -- includes -140 ps for package	480		620		850			4-9

**Table 9 — Advance Memory Buffer Component DDR2 Electrical Timing Specifications  
(Sheet 2 of 2)**

**Note: Values in the DDR2 800 column are for example only. Subject to change based on JEDEC DDR2 Specification timing closure).**

Symbol	Parameter	DDR2 800		DDR2 667		DDR2 533		Units	Fig #
		Min	Max	Min	Max	Min	Max		
System Memory Data and Strobe Signal Timings									
tDVB	DQ[63:0], CB[7:0], valid before DQS[15:0]/DQS[15:0] crossing	470		575		750		ps	4-6
tDVA	DQ[63:0], CB[7:0], valid after DQS[15:0]/DQS[15:0] crossing	470		575		750		ps	4-6
tDOPW	DQ[63:0]. CB[7:0] Output Valid Pulse Width	1.12		1.35		1.70		ns	
tSU <sub>AMB</sub>	DQ and CB Input Setup Time to DQS Crossing	-425		-530		-700		ps	4-11
tHD <sub>AMB</sub>	DQ and CB Input Hold Time After DQS Crossing	825		970		1180		ps	4-11
tWPRE <sub>AMB</sub>	DQS Write Preamble Duration	2.37	3	2.85	3.5	3.58	4.25	ns	4-12
tWPST <sub>AMB</sub>	DQS Write Postamble Duration	1.12	1.38	1.35	1.65	1.7	2.05	ns	4-13

#### 4.4.12 Reference DDR2 Interface Package Trace Lengths

The following reference package trace lengths have been incorporated into the Advance Memory Buffer timings in Table 9.

**Table 10 — Advance Memory Buffer DDR2 Package Lengths**

Signal Group	Min Length	Max Length	Units
CLK/CLK $\overline{}$	24	26	mm
Command/Address	4	20	mm
CKE, CS $\#$	9	22	mm
ODT	10	16	mm
DQS/DQS $\overline{}$ /DQ	9	13	mm

## 4.5 SMBUS Interface

**Table 11 — Recommended Operating Conditions for SMBUS Interface<sup>1</sup>**

Symbol	Parameter	Min	Typ	Max	Unit	Comments
V <sub>DDSPD</sub>	Supply voltage (SMBUS)	3.0	3.3	3.6	V	3.3v ±10%
V <sub>IL</sub>	SMBus signal input low voltage	-	-	0.8	V	
V <sub>IH</sub>	SMBus signal input high voltage	2.1	-	V <sub>DDSPD</sub>	V	
V <sub>OL</sub>	SMBus signal output low voltage	-	-	0.4	V	@I <sub>PULLUP</sub>
I <sub>LEAK-BUS</sub>	Input Leakage per bus segment	-	-	±200	uA	
I <sub>LEAK-PIN</sub>	Input Leakage per device pin	-	-	±10	uA	
I <sub>PULLUP</sub>	Current sinking, V <sub>OL</sub> = 0.4 V	4	-	-	mA	
C <sub>BUS</sub>	Capacitive load per bus segment	-	-	400	pF	
C <sub>I</sub>	Capacitance for SMBDAT or SMBCLK pin	-	-	10	pF	
V <sub>NOISE</sub>	Signal noise immunity from 10 MHz to 100 MHz	300	-	-	mV p-p	This is AC item applies to the high-power DC specification only
NOTE 1 Based on High-power SMBus DC Specification						

## 4.6 Misc I/O (1.5 CMOS Driver)

**Table 12 — Recommended Operating Conditions for RESET and BFUNC Pins**

Symbol	Parameter	Min	Typ	Max	Unit	Comments
V <sub>IH(dc)</sub>	DC HIGH-level input voltage	1.0	-	-	V	
V <sub>IL(dc)</sub>	DC LOW-level input voltage	-	-	0.5	V	
I <sub>LEAK</sub>	Input leakage	-	-	± 90	uA	

## 4.7 Thermal Diode and Analog to Digital Converter (ADC)

A thermal diode with an analog to digital converter (ADC) is required. This is required to enable closed loop thermal control from the host. The host will throttle system memory activity to reduce power. In addition, this can also be used for periodic thermal monitoring, and over-temperature shutdown.

An 8-bit register will store the temperature. The sensor measures from 0 to 127.5 degrees C measured in 0.5 degree increments in a register with values from 0 to 255. Internal analog nodes (anode, cathode, etc.) of this circuit will not be brought out to package pins to keep noise at a minimum.

The thermal sensor provides a monotonic output through the full range of component operation. The thermal sensor, and associated logic, must support Over-temperature Shutdown functionality, and a thermal trip point (i.e., TEMPHI) that guarantees operation to Tcase\_max without inadvertent shutdown<sup>1</sup>. If enabled, the system would program TEMPHI to account for sensor accuracy and required operating margin. When the thermal sensor exceeds TEMPHI, the AMB must support all OVERTEMP behaviors per section 5.1.4 Table 25.

<sup>1</sup> Tcase\_max is the Maximum Case Temperature that a specific AMB will support under normal operation. Current minimum AMB Tcase\_max as specified in AMB Component Specification is 110 °C.

Tcase Range	Sensor Accuracy to Tcase	AMB Operating Conditions	Notes
40 °C to 90 °C	$\leq \pm 10\text{ °C}$	Vcc and Vdd per 4.1.2 Table 5	1
90 °C to 124 °C	$\leq \pm 6\text{ °C}$	Vcc and Vdd per 4.1.2 Table 5	-
NOTE 1 Accuracy between 40 °C to 90 °C Tcase temperature range may be guaranteed by design without HVM testing.			

### 4.7.1 Thermal Sensor Effects on the Advanced Memory Buffer's Functional Behavior

When enabled, the results of the thermal trip points TEMPLO and TEMPMID are reported in FBD Status 0 responses following Sync commands.

If the temperature exceeds TEMPHI, errors are logged. If the TEMPHIENABLE bit in the TEMPSTAT register is set, DDR shutdown occurs and FBD links go into electrical idle mode. This over TEMPHI behavior also applies when in LAI mode. See the error chapter for a more complete description of chip behavior when TEMPHI is exceeded.

The thermal sensor does **NOT** have any effect on the behavior of the memory refresh during FBD link resets .

A temperature TEMPSTAT.INCREASING bit is also generated depending on whether the temp is greater or less than the last time the INCREASING bit was sampled. Sampling to create INCREASING bit is controlled by writes to register UPDATED. When temperature is above TEMPMID, this information also shows up in the FBDS0.Thermal\_Trip register field and in the Status response of FBD Sync commands targeted to FBDS0.

## 5 Error Handling

### 5.1 Types of Errors and Responses

#### 5.1.1 FBD Link Errors

##### 5.1.1.1 Link Initialization Errors

Table 13 shows link errors that can occur during initialization.

**Table 13 — Link Errors in Initialization**

Error	Response
Multi-lane failures - unable to achieve bit lock on at least 9 of 10 SB lanes	Never come out of Training state
Multi-lane failures - unable to achieve bit lock on at least 12 NB lanes	Never come out of Training state
NB_Data_Merge_Disable - unable to achieve bit lock (pass thru link data) but internal errors prevent receiving valid link cmds or merging data	Host sets NB_Merge_Disable bit in TS2 to cause DIMM to be in a pass-thru mode both SB and NB - act as a blind repeater 1. No attempt to decode commands, no response to link register RD/WR, generate no alerts, neither generate or merge any NB traffic 2. SMBus access enabled
Single Lane failure - SB and/or NB	Support normal initialization protocol and Fail Over mode if commanded by host

##### 5.1.1.2 Errors During Channel Operation

**Table 14 — Link Errors in Normal Operation**

Error	Response
CRC Error on SB frame “A” Command - detected by 14-bit CRC (or reduced 10-bit CRC in Fail Over mode) or CRC Error on SB data or “BC” Commands in Command Frame - detected by 22-bit CRC (or reduced 10bit CRC in Fail Over mode)	If CMDCRC error type enabled in EMASK Register 1. No command executed 2. 120-bit Raw SB Frame captured in RECFBD Error Log Registers 3. Type of error logged in FERR/NERR registers 4. Error/Alert Asserted bit set in FBD Status 0 register 5. Ignore future commands except Soft Channel Reset until Soft Channel Reset or Link Reset Received 6. Alert Frame sent continuously starting with NB frame in which returned data pattern would be sent if aborted command had been a config read. Alert patterns continue until Soft Channel Reset or Link Fast Reset received. <b>NOTE:</b> Will NOT close DRAM pages or place DRAM into Self Refresh until detection of Link Reset. Else ignore error



**Table 14 — Link Errors in Normal Operation (Continued)**

Error	Response
<p>Lose transition density on channel as detected by no Sync in within 2 times the SYNCTRAININT value (typically last 84 frames).</p> <p><b>NOTE:</b> Purpose of this error is not to detect violation of required transition density (6 out of 512) but to detect hang in the host and put DRAM into self refresh. Any corruption caused by lack of transitions will be detected by CRC violations.</p>	<p>If FEWEDGES error type enabled in EMASK Register</p> <ol style="list-style-type: none"> <li>1. No command executed in expected Sync slot</li> <li>2. 120 bit Raw SB Frame captured in RECFBD Error Log Registers</li> <li>3. Type of error logged in FERR/NERR registers</li> <li>4. Error/Alert Asserted bit set in FBD Status 0 register</li> <li>5. DDR Self Refresh FSM triggered to put DRAMs into Self Refresh</li> <li>6. Ignore future commands including Soft Channel Reset until Link Reset Received</li> <li>7. Alert Frame sent continuously starting with NB frame in which returned data pattern would be sent if aborted command had been a config read. Alert patterns continue until Link Fast Reset received.</li> </ol> <p>Else ignore error</p>
Access to unimplemented register	<p>If UNIMPLCFG error type enabled in EMASK Register</p> <ol style="list-style-type: none"> <li>1. Drop Config Write cmds</li> <li>2. Capture Addr in RECCFG register if not previously set</li> <li>3. Return 0's data if Config Read (or return -1 if Read addr to unimplemented function - though currently expect all functions to be used)</li> <li>4. UNIMPLCFG error type logged in FERR or NERR registers</li> <li>5. Error/Alert Asserted bit set in FBD Status 0 register</li> <li>6.</li> </ol> <p>Else ignore error</p>
Undefined command	Undefined commands with good CRC are ignored. This is not considered an error condition, and is not logged. Treat as reserved command or Channel NOP
TID error on config writes	<p>If the TID bit on a config write matches the value of the previous TID bit, the write is ignored. The TID bit stored in the AMB is left unchanged in this case.</p> <p>This error does not cause an alert frame, and is not logged.</p> <p>The purpose of the TID bit is to allow the host to retry a config write command following a fast reset if it does not know if it had been executed prior to an alert. If the config write had occurred the TID bit will be the same, the retried write will be ignored. If it had not occurred, the TID bit will be opposite, and the retried write to will be executed.</p>

### 5.1.2 DDR Errors

**Table 15 — DDR Errors**

Error	Response
Failure of software to achieve calibration	<p>This is detected through firmware during the calibration routine.</p> <p>Firmware should treat the DIMM as a repeater if it is an intermediate DIMM or map it out if it is the last DIMM in the chain</p>
DDR voltage does not power up	if normal FBD interface comes up, should at least act like a repeater. Does not bring down FBD channel - like above. DDR cmds directed at DIMM will fail to return valid responses

### 5.1.3 Host Protocol Errors

AMBs are not expected to detect bad protocol from the host.

**Table 16 — Host Protocol Errors**

Error	Response
Illegal combinations of commands <ul style="list-style-type: none"> <li>see Concurrent Command Delivery Rules section of the FBD Architecture and Protocol Specification</li> </ul>	AMB response to illegal command combinations is undefined
Commands to multiple AMBs to return data in the same return frame.	If multiple AMBs attempt to return data in the same frame, the host will see the data from the northern most AMB which is providing data, as it will replace any data sent from AMBs to its south. A host controller should not produce commands which would cause multiple AMBs to respond with data in the same frame. A special case can occur where Alert frames are being sent by one or more AMBs while another AMB is returning data from a command. These cases are discussed in the Architecture and Protocol spec in the Northbound Alert Frame section.

### 5.1.4 Other Errors

**Table 17 — Other Errors**

Error	Response
Overtemp - Temp > TEMPHI and overtemp enabled	If OVERTEMP error type enabled in EMASK Register <ol style="list-style-type: none"> <li>The OVERTEMP bit will be set in the FERR or NERR register as appropriate</li> <li>Error/Alert Asserted bit set in FBD Status 0 register</li> </ol> If TEMPHIENABLE set in TEMPSTAT register also <ol style="list-style-type: none"> <li>Shut down DDR channel:               <ul style="list-style-type: none"> <li>Drive CKE low to the DRAMs and float the command, address, and data signals. CKE, ODT, and clock continue to be driven. The clocks to the DRAMS may be stopped after the CKE has been registered low</li> </ul> </li> <li>The FBD interface goes to electrical idle, with the receivers shut off to reduce power.</li> <li>The core will continue to be clocked, and the Advanced Memory Buffer will respond to SMBus commands. This allows the host controller to determine the error condition</li> </ol> <b>NOTE:</b> No recovery expected, just trying to prevent Si meltdown The AMB will remain in this state until the temperature is below TEMPHI and the OVERTEMP bit is reset via SMBus or a hardware reset. Else ignore error <b>NOTE:</b> A hardware reset will place the TEMPHIENABLE bit in its default state of disabled.
Injected alert	If INJCRC error type enabled in EMASK Register <ol style="list-style-type: none"> <li>No command executed</li> <li>120 bit Raw SB Frame captured in RECFBD Error Log Registers</li> <li>Type of error logged in FERR/NERR registers</li> <li>Error/Alert Asserted bit set in FBD Status 0 register</li> <li>Ignore future commands except Soft Channel Reset until Soft Channel Reset or Link Reset Received</li> <li>Alert Frame sent continuously starting with NB frame in which returned data pattern would be sent if aborted command had been a config read. Alert patterns continue until Soft Channel Reset or Link Fast Reset received.</li> </ol> Else ignore error

**Table 17 — Other Errors (Continued)**

Error	Response
Injected error	If INJERR error type enabled in EMASK Register 1. Type of error logged in FERR/NERR registers 2. Error/Alert Asserted bit set in FBD Status 0 register Else ignore error
No REFCLK	Reset should not be released if no REFCLK present. PLL will not achieve lock, the Advanced Memory Buffer will not come out of reset.

## 5.2 Error Logging

### 5.2.1 Error Logging Procedure

There are three basic types of errors in FBD: OverTemp, Alerts and Status Only Errors. The first occurrence of errors are flagged in the FERR register. Multiple bits can be set in this register. Subsequent errors are flagged in the NERR register.

Unmasked “Alert” errors generate in-band link alert messages. Unmasked “Status Only Errors” an error bit that is returned in regularly scheduled in-band status response messages that occur following Sync commands.

There are error data logs associated with some of the errors. Once the first “Alert” error has been flagged in the FERR or NERR (and matching SB frame data logged), the log registers for that error remain locked until either 1) all “Alert” error bits in the FERR and/or NERR are cleared, or 2) a power-up reset. Once the first Unimplemented Configuration Register Access error has been flagged (and matching address logged), the log registers for that error cannot be over-written until 1) that bit in the FERR and/or NERR cleared or 2) a power-up reset.

## 5.3 Fail Over Mode Support

The Advanced Memory Buffer supports single lane Fail Over mode as described in the *FB-DMM Architecture and Protocol Specification*. This is done under host control or through the SMBus.

## 5.4 Failback to Pass-Thru

In general, the Advanced Memory Buffer attempts to minimize the number of Single Points Of Failure (SPOF) that could bring down the entire channel. Errors in any one lane can be mapped out with Fail Over. Errors on the DDR interface can be handled by disabling the DRAM interface and leaving the Advanced Memory Buffer in a repeater like mode. The goal is to allow the system (following a reset or fast reset sequence) to work around the bad DIMM and keep the DIMMs downstream in operation until there is time for system maintenance.

So, in the face of a number of error cases, an Advanced Memory Buffer in an intermediate DIMM should continue to operate in pass-thru mode so that NB and SB data are relayed to the next links in the channel with minimal functionality. Only the following parts of the Advanced Memory Buffer need to be healthy to support this mode:

- Clock inputs and PLL circuitry to generate FBD clocks
- Minimal core logic around FBD I/O enabling and reset
  - Reset generation
  - Bit lock detection.
- at least N-1 FBD lanes operational in NB and SB channels

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## 6 Transparent Mode

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### 6.1 Transparent Mode

Refer to the JEDEC publication: *FB-DIMM Draft Specification: Design for Test, Design for Validation (DFx) Specification* for information regarding Transparent Mode.

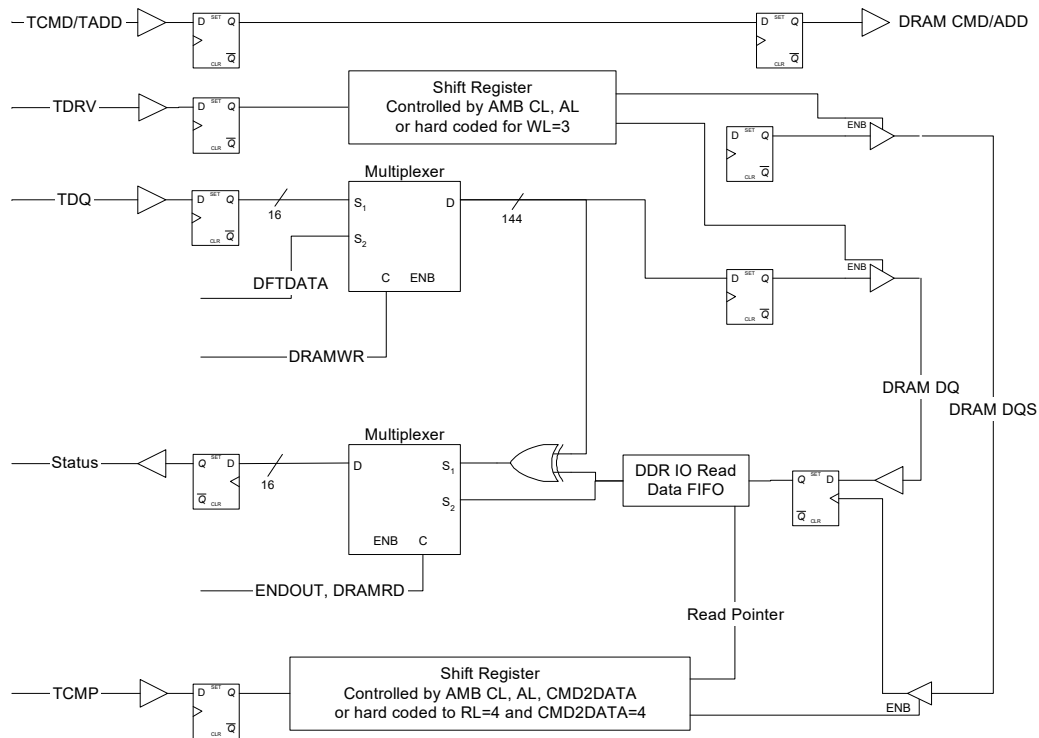
Transparent mode is designed to allow access to the DRAM behind the AMB. In this mode high speed pins are converted into low speed pins and mapped to DRAM pins. The objective is to allow the use of existing test equipment and manufacturing processes. The tester must be capable of operation at 200 MHz. Transparent mode offers potential improvements in test capacity over traditional DIMMs. In this mode, FBD requires only 60 active pins to test the DIMM.

Data from the tester is 16 bits wide at 200 MHz (single data rate). The data rate is doubled and the width halved on the way to the DRAM (by clocking out 8 bits of data on the rising edge of the clock and the remaining 8 bits on the falling edge).

The tester will drive data to be written to the DRAM on a write pass and data to be compared on a read. DRAM data and the expected data from the tester is compared in the AMB. If the actual and expected data differ the pass/fail outputs will indicate which DRAM failed.

### 6.1.1 Block Diagram

The data paths for transparent mode will bypass all link logic and normal DRAM control logic. The DDR interfaces are used intact. Figure 14 is a block diagram of the Advanced Memory Buffer part in transparent mode.



**Figure 14 — Transparent Mode Simplified Block Diagram**

### 6.1.2 Transparent Mode Signal Definitions

When the transparent mode is enabled, the FBD differential input pins designed in the Advanced Memory Buffer part become two single ended inputs. In transparent mode the FBD input pins require 0 to 500mV swing (half of the normal differential input voltage). Input slew rates should be at least 2V/ns or faster. This parameter is not critical, but it must be fast enough to be recognized by the AMB receiver. The DDR pins will operate with normal DDR2 timings and levels.

The AMB clock input pins will be used for transparent mode as well as normal mode. This also allows use of most of the existing on-chip clock distribution network.

**Table 18 — Additional Signals in Transparent Mode**

Transparent Mode Signal Name	Pin Count	Frequency	Direction	Definition
TCKE[1:0]	2	200 MHz	In	Controls CKE[1:0]{A,B}
TCS#[1:0]	2	200 MHz	In	
TODT	1	200 MHz	In	Controls both ODT[1:0]{A,B}

**Table 18 — Additional Signals in Transparent Mode (Continued)**

Transparent Mode Signal Name	Pin Count	Frequency	Direction	Definition
TRAS#	1	200 MHz	In	
TCAS#	1	200 MHz	In	
TWE#	1	200 MHz	In	Controls $\overline{WE}\{A,B\}$
TBA[2:0]	3	200 MHz	In	
TA[14:0]	15	200 MHz	In	
TDRV	1	200 MHz	In	Tester signal to drive data on writes
TCMP	1	200 MHz	In	Tester signal to compare on reads
TDQ[15:8]	8	200 MHz	In	Early data to each byte
TDQ[7:0]	8	200 MHz	In	Late data to each byte
TPF[8:0] or TDQO[15:0]	9 or 16	200 MHz	Out	Used for pass/fail (8:0) or direct access (15:0)
Sum of receivers Sum of drivers	44 16			

### 6.1.3 Transparent Mode to FBD Pin Mapping

The FBD pin mapping is shown in Table 19.

**Table 19 — Mapping of FBD Pins in Transparent Mode (Sheet 1 of 2)**

FBD Pin Name	Count	Speed	Transparent Mode Signal Name	Comment
SN[0], $\overline{SN}[0]$	2	200 MHz	TCKE[1:0]	
SN[1], $\overline{SN}[1]$	2	200 MHz	TCS#[1:0]	
SN[2], $\overline{SN}[2]$	1	200 MHz	TODT	
SN[3], $\overline{SN}[3]$	1	200 MHz	TRAS#	
SN[4], $\overline{SN}[4]$	3	200 MHz	TCAS#	
SN[5], $\overline{SN}[5]$	1	200 MHz	TWE#	
SN[13:6], [13:6]	16	200 MHz	TBA[2:0]	
PS[8]	1	200 MHz	TA[15:0]	
$\overline{PS}[8]$	1	200 MHz	TDRV	
PS[7:0]	8	200 MHz	TCMP	
$\overline{PS}[7:0]$	8	200 MHz	TDQ[15:8]	early data
			TDQ[7:0]	late data

**Table 19 — Mapping of FBD Pins in Transparent Mode (Sheet 2 of 2) (Continued)**

FBD Pin Name	Count	Speed	Transparent Mode Signal Name	Comment
SS[8:0]	9	200 MHz	TPF[8:0]	Pass/Fail mode (TRANSCFG.ENDOUT =0)
PN[13:7], SS[8:0]	16	200 MHz	TDQO[15:0]	Data output mode (TRANSCFG.ENDOUT =1)
<b>Total Pins</b>				

### 6.1.4 Clock Frequency and Core Timing

The DDR2 DRAM clock frequency is 200 to 400 MHz but core timings require several clocks (or ns) to complete.

For example on DDR2 667:

- tCL, tRP and tRCD are 4 clocks or 12 ns
- tRC is 57 ns
- tRRD is 7.5 ns

DDR2 transactions are burst-oriented, reading or writing 4 or 8 words of data across 4 or 8 clock edges. Assuming a 4 bit burst, a x8 DRAM will transfer 32 bits on successive edges of 2 DRAM clock cycles. On the tester side of the interface the same 32 bits of data is transferred, 16 bits at a time, over two DRAM cycles.

Command, address and data edges should be reasonably close to the appropriate clock edge but with some margin of error. DRAM setup and hold times are 400 to 600 ps, while the half cycle time is at least 1250 ps. As long as the data is within ¼ cycle (625 ps) of the clock edge it will not violate setup or hold. Since there will be other error terms (DIMM trace length matching, jitter etc.) it is recommended the tester be accurate to +/- 300 ps.

### 6.1.5 Transparent Mode Timing

Normally, transparent mode will use DDR2-400 timing even if the DRAM is rated for faster operation. Optionally an AMB may support operation at frequencies higher than 200 MHz.

To set up transparent mode the appropriate AMB registers should be set to AL=0, CL=4 and CMD2DATA=4. Some AMBs may default to these values, in which case programming has no effect. These values establish an internal timing relationship as illustrated in the following figures. Optionally other register values may be supported for special test cases.

Actual placement of DRAM read/write or other commands is dependent on the incoming signals, not the AMB register values. Figure 15 shows an example of a write, read, write sequence using incoming signals that correspond to WL=4 and RL=5. The timing relationships in red (normal font) are fixed relationships (established by the AMB register settings above). These edges will move together. The relationships in green (italic font) are the DRAM timings, which are under control of the tester.

Timing may be changed on the fly (e.g., in the middle of a test pattern) by changing the placement of edges from the tester. DRAM mode registers can be programmed on the fly as needed by including (E)MRS commands in the tester data stream. There is no need to change AMB settings during a test. The only exception is that DRAM BL may be changed on the fly but the data logging logic may get confused if DRAM BL does not match the BL expected by the data logger. All other DRAM settings such as AL and CL may be changed at any time.

## 6.1.5 Transparent Mode Timing (cont'd)

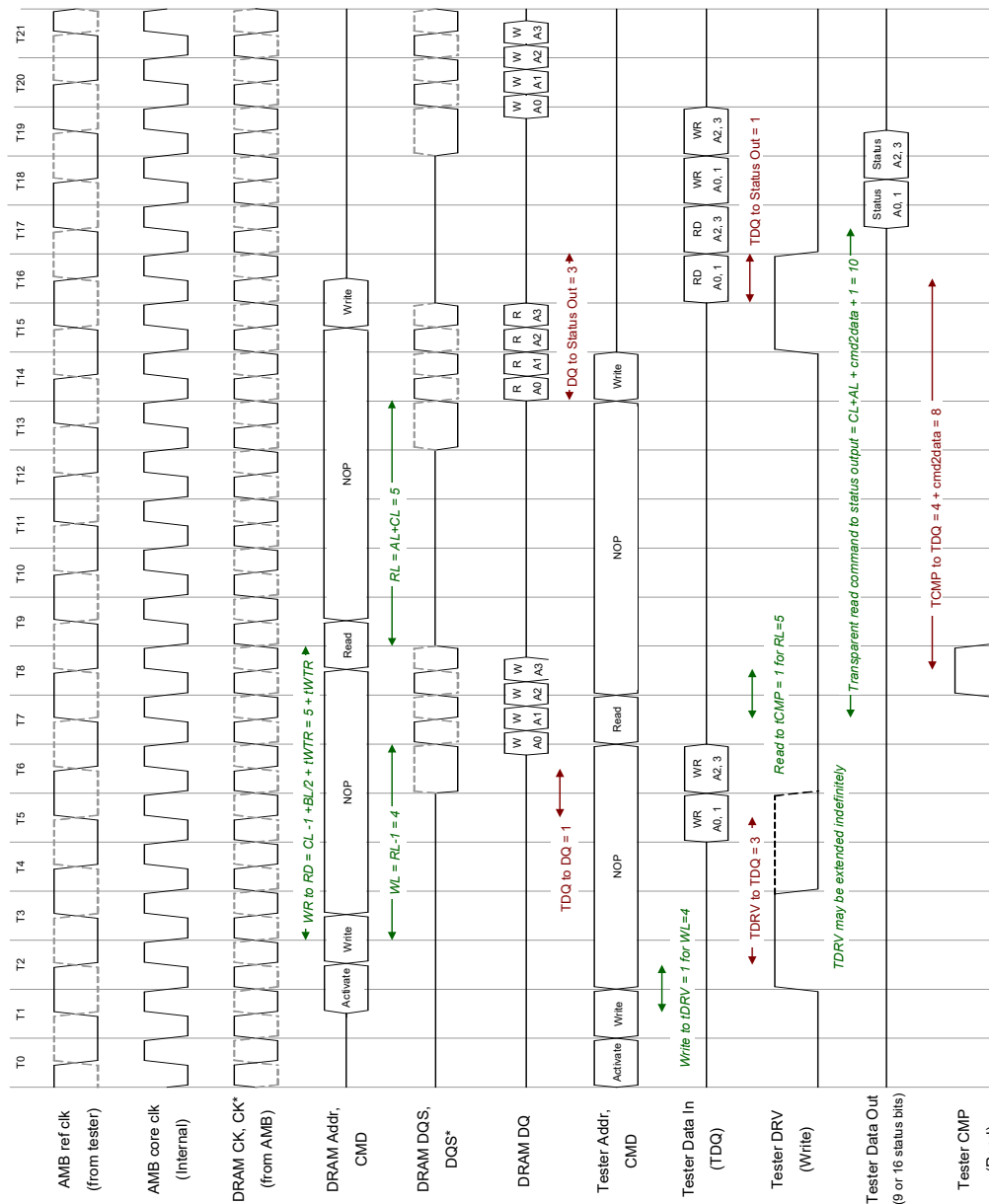


Figure 15 — Transparent Mode Timing

### 6.1.5.1 Write Timing

Figure 16 illustrates write timing with the tester set to  $WL=3, 4$ , and  $5$ . There is a constant offset of three cycles from  $TDRV$  to  $TDQ$  and one cycle from  $TDQ$  to  $DRAM DQ$ . The DRAM mode registers must, of course, be set to the appropriate timing to recognize the read. For  $BL=8$  the  $TDRV$  pulse will be 4 clocks wide rather than 2.



### 6.1.5.2 Extended Write Timing

The TDRV pulse may be extended indefinitely in cases where it is necessary to apply constant data to the DRAM pins. As long as TDRV remains asserted the AMB will continuously propagate data from the tester TDQ inputs through to the DRAM DQ pins (delayed by 1 cycle) as indicated in Figure 16.

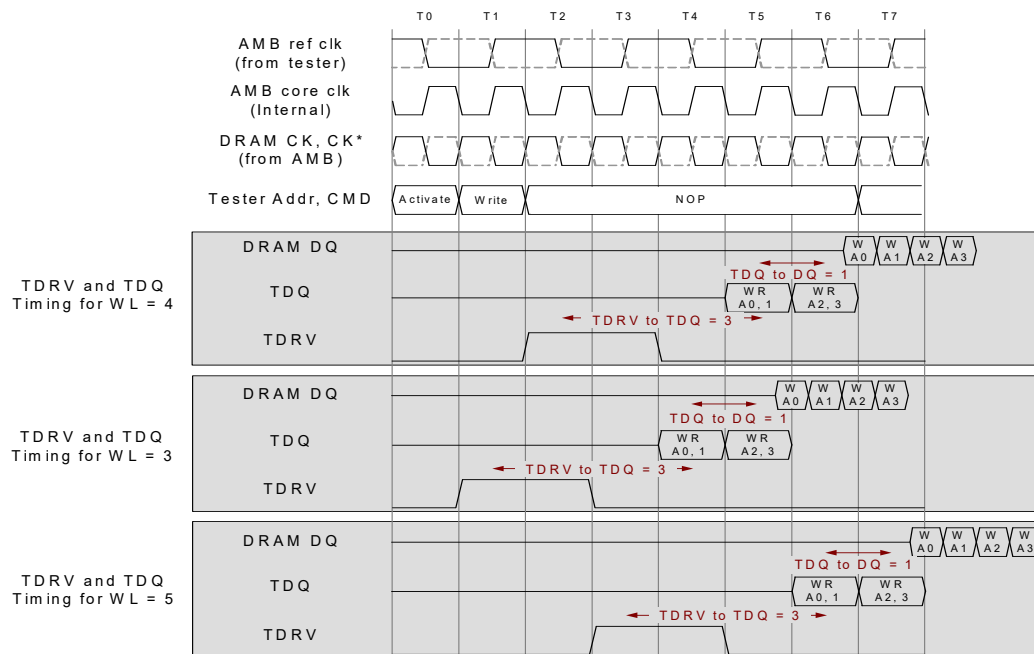


Figure 16 — Transparent Mode Write Timing

### 6.1.5.3 Read Timing

Figure 17 shows read timing with the tester set to RL=3 and RL=5. Due to complexities in the handling of read data in an AMB there is a latency of several cycles from the TDRV pulse to TDQ and test status outputs. Specifically there is a constant latency of four cycles plus the programmed CMD2DATA value from TDRV to TDQ (8 cycles total using the AMB settings above) and one cycle from TDQ to DRAM DQ. An AMB may support shorter latencies but this is not required.

TCMP is latched on the rising edge of core clock. This initiates the read inside the AMB. In most cases the AMB will latch DRAM read data slightly before TDQ data is needed. The reason is most AMBs will load DDR data into a queue in the DRAM domain and unload the data on a core clock edge. TDQ is typically not needed until the DRAM data is in the core. The comparison of actual and expected data and propagation back to the tester will occur on the next core clock edge.

The timings below are for BL=4. When testing BL=8 the TCMP pulse should be 3 clocks wide rather than 1. Tester DQ data, DRAM data and the status outputs will be extended appropriately to cover the burst length.

6.1.5.3 Read Timing (cont'd)

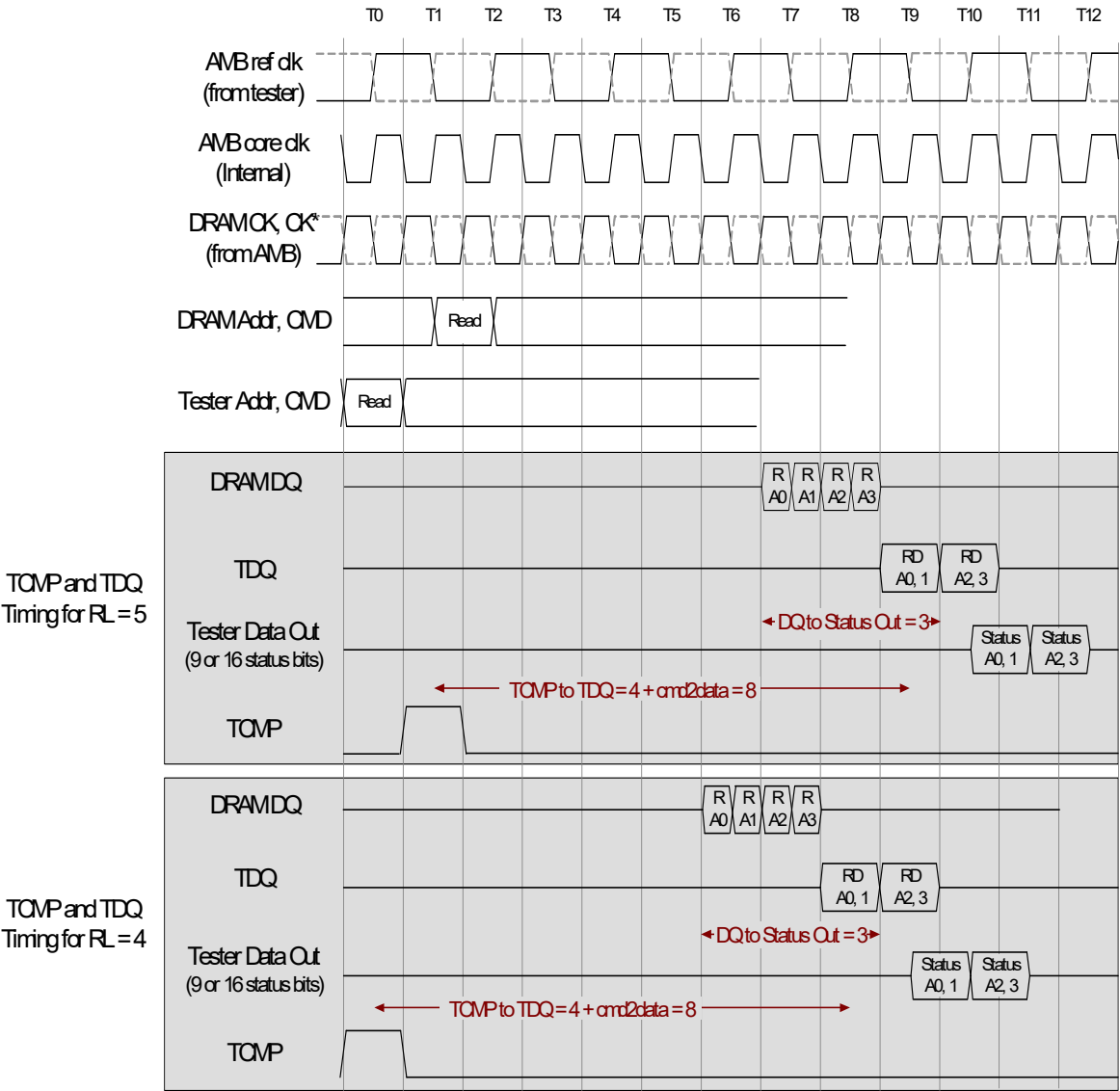


Figure 17 — Transparent Mode Read Timing

### 6.1.5.3 Read Timing (cont'd)

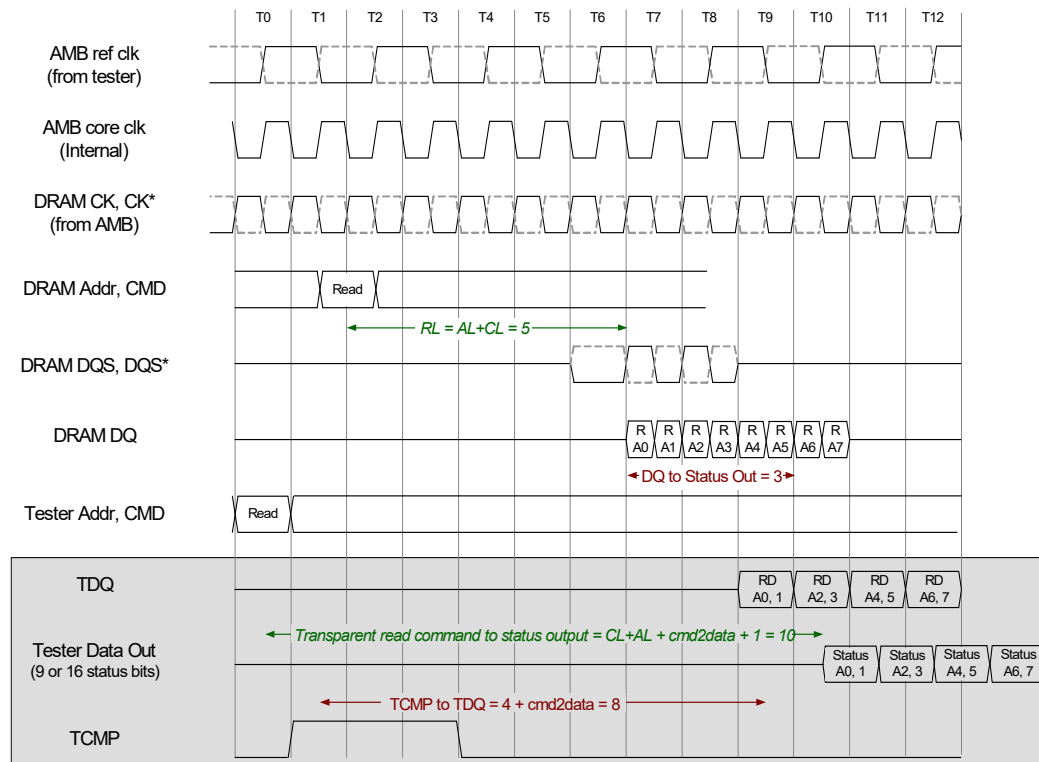


Figure 18 — BL=8 Read Timing

### 6.1.6 Error Reporting

By default, the status pins will be the xor of actual data from the DRAM and expected data from the tester. The AMB also stores 144 bits of DQ data. If the LGFBITS control bit is cleared the 144 bits of data will be actual data read from the DRAM. Otherwise the result of the data compare is stored. In either case the tester must still provide expected data for the AMB to properly set the status pins.

Normally the test will stop when an error occurs. It is the responsibility of the tester or test program to track errors, read error registers and stop or continue as appropriate. This may require multiple iterations of the same test to execute, collect data and re-start the test.

#### 6.1.6.1 Multiple Failures

There are some implications if multiple failures occur in the same DRAM burst. Three control register bits determine how these failures should be captured. If the log first fail (LGFFAIL) bit is set, the AMB will record only the first failure in a burst. When the bit is cleared (default), the AMB will record the last failure at the burst position matching the burst position (BSTPOS) setting. If the LGFFAIL bit is set and an error is logged, no further logging will occur until the bit is cleared.

a) If a failure is detected only in one half of the burst (first and second or third and fourth data words), the error pins will indicate which DRAM or DRAMs failed. The error register will indicate which data lines failed and in which data words.

### 6.1.6.1 Multiple Failures (cont'd)

b) If a failure is detected in both halves of the burst (data word 1 or 2 and words 3 or 4), data from the second failure will overwrite data from the first failure. By default this is prevented by the log fail bit. The error pins will continue to operate correctly. If it is desired to collect data from a specific portion of the burst the burst position bits can be used to select an appropriate burst position to record. For a 4 bit burst it is possible to select data from the first or second half of the burst. For an 8 bit burst there are four positions to choose from. These mappings are illustrated in Table 20.

**Table 20 — Mapping of Burst Position Bits to Error Capture**

Log First Fail	Burst Position		BL=4			
	Bit1	Bit0	1	2	3	4
1	x	x	144 bits*		or 144 bits*	
0	0	0	144 bits			
0	0	1			144 bits	

Log First Fail	Burst Position		BL=8								
Bit0	Bit1	Bit0	1	2	3	4	5	6	7	8	
1	x	x	144 bits*		or 144 bits*		or 144 bits*		or 144 bits*		
0	0	0	144 bits								
0	0	1				144 bits					
0	1	0						144 bits			
0	1	1								144 bits	

\* the first failure will be saved in whatever burst position it occurs

### 6.1.6.2 Direct Access - Testing of Individual DRAMs

In certain cases, it is desirable to test one or two DRAMs. Transparent mode allows direct access to a single x8 or two x4 DRAMs. In this mode 8 DDR DQ pins are demultiplexed onto 16 SDR status pins, providing 16 bit input data path (on TDQ) and a 16 bit output data path on the status pins.

The transparent mode configuration register has one bit (ENDOUT) to enable this mode. On reads, the DRAMRD bits will select the bytes of DRAM data to be presented on the status pins. On writes the DRAMWR bits select a DRAM to receive data from the TDQ bus. A separate register holds 8 bits of default data to be applied to non-selected DRAMs in the early/even cycles and another 8 bits for late/odd cycles. The mapping of these bits to DQ selection is illustrated in Table 21.

### 6.1.6.2 Direct Access - Testing of Individual DRAMs (cont'd)

**Table 21 — Selection of 8 Bit Data Paths when ENDOUT is Set**

DRAM RD/WR	DQ	Early Data DQ Byte	Late Data DQ Byte
0xF (DRAM WR only)	all bytes		
8	71:64	8	17
7	63:56	7	16
6	55:48	6	15
5	47:40	5	14
4	39:32	4	13
3	31:24	3	12
2	23:16	2	11
1	15:8	1	10
0	7:0	0	9

DRAMWR is the byte of data bus selected to receive transparent write data, and byte of data bus to be compared against transparent read data. DRAMWR allows a setting of 0xF (all ones) which sends the TDQ input data to all DQ bytes. DRAMRD is the byte of data bus selected to be output on transparent data/status pins when ENDOUT bit is set.

### 6.1.7 Transparent Mode IO Specifications

Table 22 lists the specifications for transparent mode input and output pins.

**Table 22 — Transparent Mode FB-DIMM Interface Signaling Specifications**

	Minimum	Maximum	Units
I/O voltage swing	0	500	mV
Input slew rate	2	-	V/ns
Input to refclk setup time	3000	-	ps
Input to refclk hold time	1000	-	ps
Status output valid to refclk time	-1000	+1000	ps
Vref	200	300	mV
Vil (DC)	-300	200	mV
Vil (AC)	-300	150	mV
Vih (DC)	300	900	mV
Vih (AC)	350	900	mV
Voh	400	-	mV
Vol	-	100	mV
Ioh <sup>1</sup>	8	-	mA
Iol <sup>2</sup>	12	-	mA
NOTE 1 Ioh: current into a 50-ohm external load to ground, with on-die transmitter termination enabled			
NOTE 2 Iol: current into a 50-ohm external load to 1.5 V supply rail, with on-die transmitter termination enabled			

## 6.1.8 IO Implementation Guidelines

### 6.1.8.1 Dedicated Receivers

Simple one-stage receivers for the transparent mode have been added in parallel to the existing high-speed sampling receivers. The latter can be turned off during transparent mode, as well as the DRC and the phase interpolator, to save power and avoid noise. An internal VREF set to 0.25 V will be used, so the tester signals should oscillate between 0 and 0.5 V. The transparent mode RX should be turned off during normal mode, so as to save power/avoid noise.

### 6.1.8.2 Common Clock Scheme

To avoid costly implementations using strobes and FIFOs, a common clock scheme is followed, implemented in the core, where the data capture flops reside. Since transparent mode data signals from the tester are all in phase with the 100 MHz system clock, the clock used for the capture flops has to be aligned with the external system clock (or slightly delayed, to account for the propagation delay difference between data receivers and clock receiver).

Aligning core clock and external clock can be done using the HVM mode circuitry included in the PLL. The HVM clock tree will have to feed the capture flops, and one of its leaves has to be fed back to the PLL, in order to achieve adequate synchronization.

### 6.1.8.3 Tester Interface Clock and Data Routing

The following uncertainties have to be factored in:

- Tester board (TIU) trace mismatches
- Package trace mismatches
- FBD low speed RX propagation delay variations due to PVT
- Set up and hold of capture flops (typically <350 ps depending on process, voltage and temperature)
- Clock synchronization mismatch, core clock PLL and tree jitter (approximately +/-200 ps)

At 200 MHz, there is a 5 ns data window. The potential FBD low speed receiver variation is approximately 300ps propagation variation over process, voltage and temperature. Package and tester interface mismatches are not expected to exceed 200 ps. Flop setup variation should also be less than 200 ps. After removing 400ps for clock uncertainties leaves 3.9 ns margin. While this is plenty of margin, some amount of trace matching should be done on the tester interface to minimize skew.

### 6.1.8.4 Outgoing Control Signals

Only the TX+ pin should connect to the tester. The data on TX- can be discarded (it will toggle at the same rate as TX+).

Terminating TX+ on the tester should be a given, as every tester offers this capability. Terminating TX- could be done on the tester, by having a TIU (tester board) with a route and a tester connection allocated for it. It may be cheaper to just have a 50 ohm resistor tied to ground on the TIU itself, from the TX- pins.

To avoid the crossing clock domains from core clock to FBD fast clocks, the transparent mode data flows directly through the Analog Front-end Unit of the TX.

### 6.1.8.5 Usage Models

#### 6.1.8.5.1 Host Side Usage

TX: The transmitters are set the same as in normal operation (bias on, enable termination, etc.).

RX: RX+ and RX- signals will be independent. Incoming data will free-flow through the I/O (no flops). The routing distance from transparent\_rxout pins should be the same for all capture flops. All these flops should be clocked by the dedicated HVM clock.

#### **6.1.8.5.2 Tester Side Usage**

The tester interface should have trace-matched data signals, to avoid skews  $> 1\text{ns}$ . The tester should have 50 ohm terminations to ground for all TX pins in use (on-tester termination can be used where applicable). The tester should enable 50 ohm terminations to ground for all the signals sent to RX pins. This will guarantee reasonable signal integrity.

### **6.2 Transparent Mode Control and Status Registers**

In transparent mode, CSRs will be accessed and programmed through SMBus. See Chapter 12, “Configuration Registers,” for register descriptions.

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## 7 SMBus Interface

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The Advanced Memory Buffer has configuration registers that provide flexibility and allow for testing and optimization of the chip. Upon system reset (RESET#), configuration registers are reset to predetermined default states, representing the minimum feature set required to successfully bring up a nominal channel. It is expected that the BIOS will properly determine and program the optimal configuration settings.

For all of these registers, the Advanced Memory Buffer supports register access mechanisms through SMBus as well as through in-band channel commands.

### 7.1 System Management Access

System Management software in the platform can initiate system management access to the configuration registers. This can be done through SMBus accesses.

The mechanism for the Server Management (SM) software to access configuration registers is through a *SMBus Specification*, Rev. 2.0-compliant target port. Advanced Memory Buffer components contain this target port and allow access to the configuration registers.

SMBus operations are made up of two major steps: (1) writing information to registers within each component and (2) reading configuration registers from each component. The following sections will describe the protocol for an SMBus controller to access an Advanced Memory Buffer component's internal configuration registers. Refer to the *SMBus Specification*, Rev. 2.0 for the bus protocol, timings, and waveforms.

#### 7.1.1 SMBus 2.0 Specification Compatibility

The principal requirement from the SMBus 2.0 specification is support of the “high power” bus electrical specifications described in the layer 1 (Physical layer) chapter.

For the simple register access requirements of FBD, no layer 2 (Link layer) or layer 3 (Network layer) extensions provided by the 2.0 specification are used. In particular, there is no support for Address Resolution Protocol (ARP) since FBD is using fixed addresses. Additionally, only a subset of the network packet protocols described in the specification are needed and these are described below.

AMB's are required to support read and write transactions without requiring clock stretching in order to simplify host controller requirements. For similar reasons, AMB's should not control SMBus transactions in normal operation.

#### 7.1.2 Supported SMBus Commands

The Advanced Memory Buffer components SMBus Rev. 2.0 target ports support register reads and writes built out of the following SMBus primitive commands:

Block Write      Byte Write

Block Read      Byte Read

The target address for each primitive SMBus transaction are determined from the SA pins.

- For normal FBD DIMMs:
  - Target Address[6:3] = 4'b1011
  - Target Address[2:0] = SA[2:0]



### 7.1.2 Supported SMBus Commands (cont'd)

- For repeaters or LAI AMBs:
  - Target Address[6:3] = 4'b0011
  - Target Address[2:0] = SA[2:0]

Each SMBus transaction has an 8-bit command driven by the controller. The format for this command is illustrated in Table 23.

**Table 23 — SMBus Command Encoding**

7	6	5	4	3:2	1:0
Begin	End	Rsvd	PEC_en	Internal Command: 00 - Read DWord 01 - Write Byte 10 - Write Word 11 - Write DWord	SMBus Command: 00 - Byte 01 - <i>Rsvd</i> 10 - Block 11 - <i>Rsvd</i>

The *Begin* bit indicates the first transaction of a read or write sequence.

The *End* bit indicates the last transaction of a read or write sequence.

The *PEC\_en* bit enables the 8-bit PEC generation and checking logic.

The *Internal Command* field specifies the internal command to be issued by the SMBus target logic. Note that the Internal Command must remain consistent (i.e., not change) during a sequence that accesses a configuration register. Operation cannot be guaranteed if it is not consistent when the command setup sequence is done.

The *SMBus Command* field specifies the SMBus command to be issued on the bus. This field is used as an indication of the length of transfer so the target knows when to expect the PEC packet (if enabled).

Reserved bits should be written to zero to preserve future compatibility.

### 7.1.3 FBD AMB Register Access Protocols

Sequences of these basic commands will initiate internal accesses to the component's configuration registers.

Each configuration read or write first consists of an SMBus write sequence which initializes the register's address. The term sequence is used since these variables may be written with a single block write or multiple byte writes. Once these parameters are initialized, the SMBus controller can initiate a read sequence (which performs a configuration read) or a write sequence (which performs a configuration write).

### 7.1.3 FBD AMB Register Access Protocols (cont'd)

**Table 24 — SMBus Protocol Addressing Fields**

Address Field Name	Bits	Description
Reserved	7:0	Reserved - AMB may alias all these addresses to 00h
Dev	4:0	Reserved - AMB may alias all these addresses to 00h
Function	2:0	Function Address
Reg_Num[15:]	7:0	Reserved - AMB may alias all these addresses to 00h
Reg_Num[7:0]	7:0	Register Address within Function

#### 7.1.3.1 Configuration Register Read Protocol

Configuration reads are accomplished through an SMBus write(s) and later followed by an SMBus read. The write sequence is used to initialize the Bus Number, Device, Function, and Register Number for the configuration access. The writing of this information can be accomplished through any combination of the supported SMBus write commands (Block, Byte). The *Internal Command* field for each write should specify Read DWord.

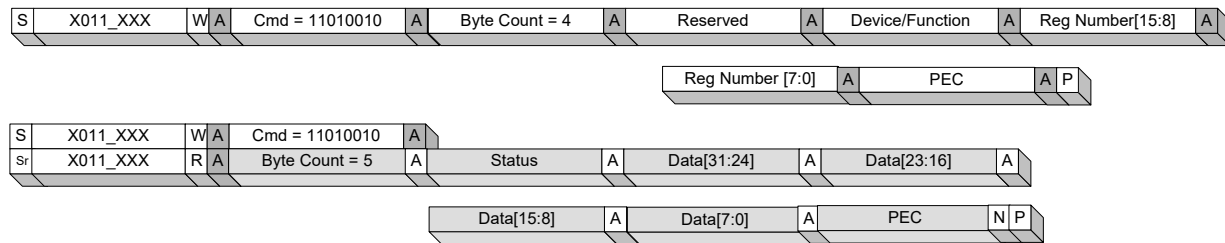
After all the information is set up, the last write (*End* bit is set) initiates an internal configuration read. If an error occurs during the internal access, the last write command will receive a NACK. A status field indicates abnormal termination and contains status information such as target abort, controller abort, and time-outs. The status field encoding is defined in Table 25.

**Table 25 — Status Field Encoding for SMBus Reads**

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Internal Target Abort
3:1	Reserved
0	Successful

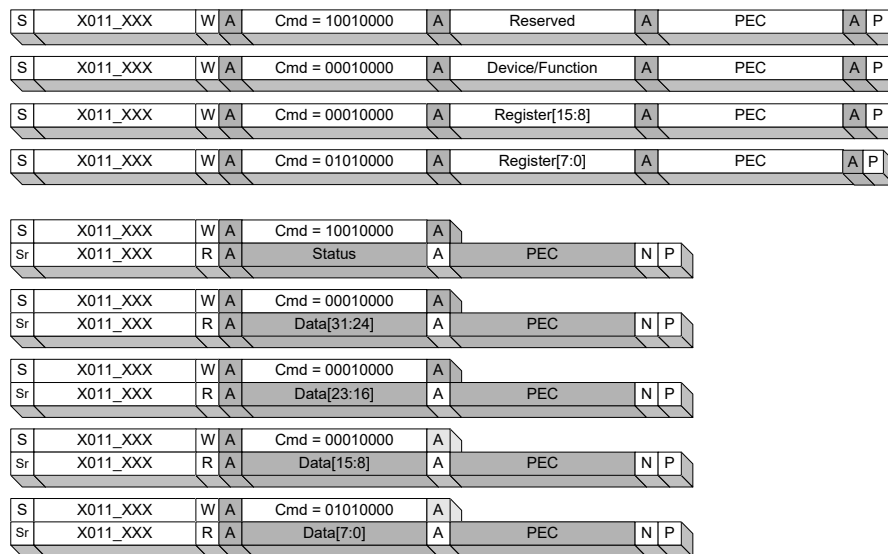
Examples of configuration reads are illustrated in Figure 19. All of these examples have PEC (Packet Error Code) enabled. If the controller does not support PEC, then bit 4 of the command would be cleared and there would not be a PEC phase. For the definition of the diagram conventions below, refer to the *SMBus Specification*, Rev. 2.0. For SMBus read transactions, the last byte of data (or the PEC byte if enabled) is NACKed by the controller to indicate the end of the transaction. For diagram compactness, “Register Number[]” is also sometimes referred to as “Reg Number” or “Reg Num”.

### 7.1.3.1 Configuration Register Read Protocol (cont'd)



**Figure 19 — SMBus Configuration Read (Block Write / Block Read, PEC Enabled)**

Figure 20 uses byte reads.



**Figure 20 — SMBus Configuration Read (Write Bytes / Read Bytes, PEC enabled)**

### 7.1.3.2 Configuration Register Write Protocol

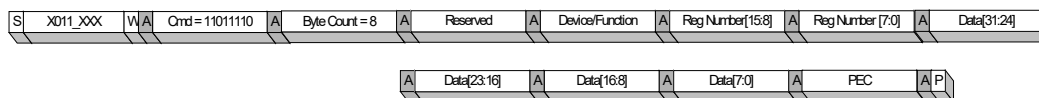
Configuration writes are accomplished through a series of SMBus writes. As with configuration reads, a write sequence is first used to initialize the Bus Number, Device, Function, and Register Number for the configuration access. The writing of this information can be accomplished through any combination of the supported SMBus write commands (Block, Byte).

On SMBus, there is no concept of byte enables. Therefore, the Register Number written to the target is assumed to be aligned to the length of the Internal Command. In other words, for a Write Byte internal command, the Register Number specifies the byte address. For a Write DWord internal command, the two least-significant bits of the Register Number are ignored. This is different from PCI where the byte enables are used to indicate the byte of interest.

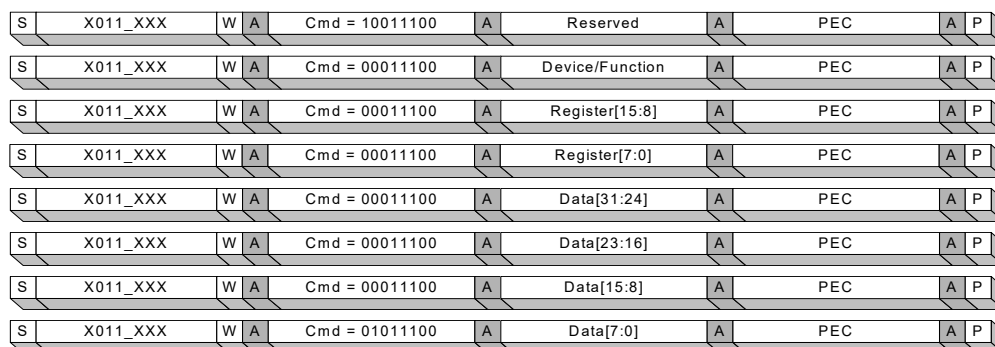
After all the information is set up, the SMBus controller initiates one or more writes which sets up the data to be written. The final write (*End* bit is set) initiates an internal configuration write. If an error occurred, the SMBus interface NACKs the last write operation just before the stop bit.

### 7.1.3.2 Configuration Register Write Protocol (cont'd)

Examples of configuration writes are illustrated in Figure 21 through Figure 24. For the definition of the diagram conventions in these figures, refer to the *SMBus Specification*, Rev. 2.0.



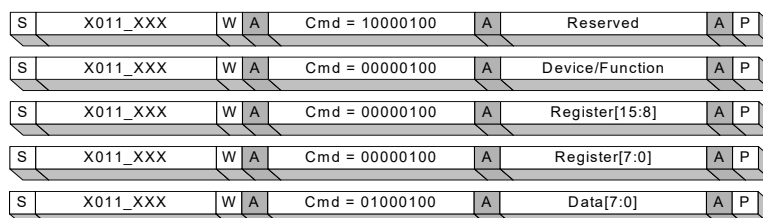
**Figure 21 — SMBus Configuration Double Word Write (Block Write, PEC Enabled)**



**Figure 22 — SMBus Configuration Double Word Write (Write Bytes, PEC Enabled)**



**Figure 23 — SMBus Configuration Word Write (Block Write, PEC Disabled)**



**Figure 24 — SMBus Configuration Byte Write (Write Bytes, PEC Disabled)**

### 7.1.4 SMBus Error Handling

The SMBus target interface handles two types of errors: internal and PEC. These errors manifest as a Not-Acknowledge (NACK) for the read command (*End* bit is set). If an internal error occurs during a configuration write, the final write command receives a NACK just before the stop bit. If the controller receives a NACK, the entire configuration transaction should be reattempted.

If the controller supports packet error checking (PEC) and the PEC\_en bit in the command is set, then the PEC byte is checked in the target interface. If the check indicates a failure, then the target will NACK the PEC packet.

### 7.1.5 SMBus Resets

#### 7.1.5.1 SMBus Transactions during FBD Link Fast Reset

When the FBD link transitions into Electrical Idle (disable state) from an active state, this causes a “fast” reset of all non-sticky registers in the AMB. SMB transactions underway during a “fast” reset will not complete normally.

Generally, this is not a problem since SMBus accesses are only required prior to initial link turn-on or for diagnostic access when a link can not be initialized. It is the host’s responsibility to monitor for SMBus transactions during a fast reset and retry these transactions when the link is stable.

Generally, an interrupted transaction will result in the AMB as target not properly acknowledging the Controller. This protects write transactions. However, if a read transaction has proceeded to the point where the target no longer acknowledges the controller, read data can be lost when the SMBus state machine is reset. If PEC is enabled, this data loss will be detected as a PEC error.

The host restricting usage of SMBus to when the link is idle or monitoring “fast resets” and retrying transactions that are interrupted is the safest SMBus access method.

#### 7.1.5.2 SMBus Interface State Machine Reset

The target interface state machine can be reset by the controller in two ways:

- The controller holds SCL low for 25 ms cumulative. Cumulative in this case means that all the “low time” for SCL is counted between the Start and Stop bit. If this totals 25 ms before reaching the Stop bit, the interface is reset.
  - Timing is set up to be 25 ms for DDR2-800 and may scale up at lower frequencies
    - \* 30 ms at DDR2-667
    - \* 37.5 ms at DDR2-533
- The controller holds SCL continuously high for 50us.
  - Timing is set up to be 50us for DDR2-800 and may scale up at lower frequencies
    - \* 60  $\mu$ s at DDR2-667
    - \* 75  $\mu$ s at DDR2-533

#### 7.1.5.3 SMBus Transactions during Hard Reset

Since the configuration registers are affected by the reset pin, SMBus controllers will NOT be able to access the internal registers while the system is reset.

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## 8 Clocking

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### 8.1 Advanced Memory Buffer Clock Domains

There are three main clock domains in the Advanced Memory Buffer. The FBD link domain is a 12x multiple of the core clock. The DDR data-rate domain is 2x the core clock. The core domain frequency equals the DDR command-rate, and is a 2x multiple of the external reference clock. The ratio between these domains remains fixed.

### 8.2 PLL Clocks

The PLL receives a reference clock at  $1/2X$ , where  $X$  is the DDR command frequency. The PLL generates the internal clocks.

### 8.3 Reference Clock

A low-jitter differential reference clock (REFCLK) is routed to the host and each DIMM from a common clock source on the system board. This reference clock uses HCSL (High-Speed Current Steering Logic) signaling and its detailed requirements are documented in the FB-DIMM Draft Specification: High Speed Differential P2P Link at 1.5 V[ref tbd]. The Advanced Memory Buffer uses the reference clock to generate internal buffer clocks and to generate the clocks to the DRAMs located on each DIMM. The frequency of the reference clocks (133 to 200 MHz) is one half the frequency of the DRAM base clock (267 to 400 MHz), i.e., it is one half the command-rate of the DRAM devices located behind the Advanced Memory Buffer. For example, for DDR2 667 DRAM devices the reference clock frequency would be 167 MHz. The reference clock is the basis for the various Core, FBD, and DDR internal clocks.

It is a requirement for the FBD channel to operate in the presence of Spread Spectrum Clocking (SSC), which is commonly used to reduce EMI. The reference clocks for FBD have to meet a jitter specification.

The reference clocks to the host and each DIMM are mesochronous, i.e., they have an unknown but fixed phase relationship to each other or the memory channel. This simplifies PCB routing since no precise length matching is required. However an upper bound for the clock length mismatch is necessary since the maximum phase difference between the data sent out with the transmitter clock and the receiver clock needs to be limited in the presence of SSC. It is required that all the reference clocks for a given FBD channel originate from a single clock source, e.g., a common clock synthesizer or clock oscillator, and travel through the same jitter spectrum modifying components (e.g., PLL clock buffer) thereby ensuring that there is no frequency mismatch or frequency drift between FBD agents.

The PLL will also operate with the REFCLK at 100 MHz during special transparent mode testing. Since there is no high speed link operation, there can be looser requirements for jitter and no SSC.

### 8.4 FBD Lane Frame Clocks

Each FBD I/O lane also sources a frame clock at core frequency that is matched to the parallel data sourced by the lane. These are used during initialization to capture data in training sequences and to align data across the link.

### 8.5 Clock Ratios

The core, DDR and FBD link clock domains are fixed in a 1:2:12 ratio. The SMBus asynchronous subsystem need not scale. The supported clock ratios are shown in Table 26.

## 8.5 Clock Ratios (cont'd)

**Table 26 — Advanced Memory Buffer Clock Ratios**

FBD Link Data Rate	DDR Data Rate	Core Frequency	Ref Clk <sup>1</sup>	FBD Link : Core	Core : DDR
3.2 Gb/s	533 Mb/s	266 MHz	133 MHz	12 : 1	1 : 2
4.0 Gb/s	666 Mb/s	333 MHz	167 MHz	12 : 1	1 : 2
4.8 Gb/s	800 Mb/s	400 MHz	200 MHz	12 : 1	1 : 2
NOTE 1 The clock tolerance for the reference clock is -5%, +0.05%. This is reflected in Table 3-1 of the “FB-DIMM Draft Specification: High Speed Differential PTP Link at 1.5 V”. Because of this, the FBD Link Data Rate will support the same tolerance (i.e., -5% and +0.05%) as well.					

## 8.6 DDR DRAM Clock Support

The DDR command clocks (CLK[3:0],  $\overline{\text{CLK}}$ [3:0]) are generated by the Advanced Memory Buffer. They operate at 1X the core frequency for DDR2.

The write strobes operate at the same frequency as the CLK/ $\overline{\text{CLK}}$  signals. Write data and check bits are aligned to both the rising and falling edges of the write strobe.

The source-synchronous read strobes operate at the same rates as the write strobes. Each read strobe will be individually aligned with its portion of the data and check-bits.

## 8.7 Clock Pins

**Table 27 — Clock Pins**

Pin Name	Pin Description
SCK	Advanced Memory Buffer clock
SCK	Advanced Memory Buffer clock (Complement)
VCCAPLL	analog power supply for PLL
VSSAPLL	analog ground for PLL
SCL	SMBus clock
CKE[1:0]{A,B}	DDR clock enables
CLK[3:0]	DDR clocks
$\overline{\text{CLK}}$ [3:0]	DDR clocks (Complements)
DQS[17:0]	DDR data/check-bit strobes
$\overline{\text{DQS}}$ [17:0]	DDR data/check-bit strobes (Complements)

## 8.8 PLL Requirements

### 8.8.1 Jitter

See the FB-DIMM Draft Specification: High Speed Differential P2P Link at 1.5 V[ref tbd] for more details.

### **8.8.2 PLL Bandwidth Requirements**

See the FB-DIMM Draft Specification: High Speed Differential P2P Link at 1.5 V[ref tbd] for more details.

### **8.8.3 External Reference**

See the FB-DIMM Draft Specification: High Speed Differential P2P Link at 1.5 V[ref tbd] for more details.

### **8.8.4 Spread Spectrum Support**

See the FB-DIMM Draft Specification: High Speed Differential P2P Link at 1.5 V[ref tbd] for more details.

## **8.9 Analog Power Supply Pins**

Separate filtered power pins are available for use by a PLL if needed.

Warning: The filters are NOT to be connected to board Vss. The ground connection of the filters will be routed through the package and grounded to on-die Vss.



## 9 Pin Descriptions

### 9.1 Pin Description

**Table 28 — Buffer Signal Types**

Buffer Direction	Description
I	Input signal
O	Output signal
A	Analog
I/O	Bidirectional (input/output) signal
NC	No Connect.

**Table 29 — Pin Description**

Signal	Type	Description
<b>Channel Interface</b>		
PN[13:0]	O	<b>Northbound Output Data:</b> High speed serial signal. Read path from AMB toward host on primary side of the DIMM connector.
$\overline{\text{PN}}[13:0]$	O	Northbound Output Data Complement
SN[13:0]	I	<b>Northbound Input Data:</b> High speed serial signal. Read path from the previous AMB toward this AMB on secondary side of the DIMM connector.
$\overline{\text{SN}}[13:0]$	I	Northbound Input Data Complement
PS[9:0]	I	<b>Southbound Input Data:</b> High speed serial signal. Write path from host toward AMB on primary side of the DIMM connector.
$\overline{\text{PS}}[9:0]$	I	Southbound Input Data Complement
SS[9:0]	O	<b>Southbound Output Data:</b> High speed serial signal. Write path from this AMB toward next AMB on secondary side of the DIMM connector. These output buffers are disabled for the last AMB on the channel.
$\overline{\text{SS}}[9:0]$	O	Southbound Output Data Complement
FBDRES	A	External precision resistor connected to VCC. On-die termination calibrated against this resistor.
<b>DRAM Interface</b>		
CB[7:0]	I/O	Check bits
DQ[63:0]	I/O	Data
DQS[17:0]	I/O	<b>Data Strobe:</b> DDR2 data and check-bit strobe.
$\overline{\text{DQS}}[17:0]$	I/O	<b>Data Strobe Complement:</b> DDR2 data and check-bit strobe complements.
A0A-A15A, A0B-A15B	O	<b>Address:</b> Used for providing multiplexed row and column address to SDRAM.

**Table 29 — Pin Description (Continued)**

Signal	Type	Description
BA0A-BA2A, BA0B-BA2B	O	<b>Bank Active:</b> Used to select the bank within a rank.
$\overline{\text{RASA}}$ , $\overline{\text{RASB}}$	O	<b>Row Address Strobe:</b> Used with $\overline{\text{CS}}$ , $\overline{\text{CAS}}$ , and $\overline{\text{WE}}$ to specify the SDRAM command.
$\overline{\text{CASA}}$ , $\overline{\text{CASB}}$	O	<b>Column Address Strobe:</b> Used with $\overline{\text{CS}}$ , $\overline{\text{RAS}}$ , and $\overline{\text{WE}}$ to specify the SDRAM command.
$\overline{\text{WEA}}$ , $\overline{\text{WEB}}$	O	<b>Write Enable:</b> Used with $\overline{\text{CS}}$ , $\overline{\text{CAS}}$ , and $\overline{\text{RAS}}$ to specify the SDRAM command.
$\overline{\text{CS0A}}-\overline{\text{CS1A}}$ , $\overline{\text{CS0B}}-\overline{\text{CS1B}}$	O	<b>Chip Select:</b> Used with $\overline{\text{CAS}}$ , $\overline{\text{RAS}}$ , and $\overline{\text{WE}}$ to specify the SDRAM command. These signals are used for selecting one of two SDRAM ranks. $\overline{\text{CS0}}$ is used to select the first rank and $\overline{\text{CS1}}$ is used to select the second rank.
CKE0A-CKE1A, CKE0B-CKE1B	O	<b>Clock Enable:</b> DIMM command register enable.
ODT0A, ODT0B	O	<b>DIMM On-Die-Termination:</b> Dynamic ODT enables for each DIMM on the channel.
CLK[3:0]	O	<b>Clock:</b> Clocks to DRAMs. CLK0 and CLK1 are always used. CLK2 and CLK3 are optional and may be disabled when not required.
CLK[3:0]	O	<b>Clock Complement:</b> Clocks to DRAMs.
<b>DDR Compensation</b>		
DDRC_C14	A	<b>DDR Compensation Common:</b> Common return (ground) pin for DDRC_B18 and DDRC_C18
DDRC_B18	A	DDR Compensation Ball Resistor connected to Compensation Common above
DDRC_C18	A	DDR Compensation Ball Resistor connected to Compensation Common above
DDRC_B12	A	DDR Compensation Ball Resistor connected to VSS
DDRC_C12	A	<b>DDR Compensation Ball</b> Resistor connected to VDD
<b>Clocking</b>		
SCK	I	<b>AMB Clock:</b> This is one of the two differential reference clock inputs to the Phase Locked Loop in the AMB core. Phase Locked Loops in the AMB will shift this to all frequencies required by the core, DDR channels, and FBD Channel.
SCK	I	<b>AMB Clock Complement:</b> This is the other differential reference clock input to the Phase Locked Loop in the AMB core. Phase Locked Loops in the AMB will shift this to all frequencies required by the core, DDR channels, and FBD Channel.
PLLTSTO	O	<b>PLL Clock Observability Output:</b> This pin can be used to observe VCO, reference clock, core clock, etc. For system debug and design characterization.
VCCAPLL	A	<b>VCC:</b> PLL Analog Voltage for the core PLL
VSSAPLL	A	<b>VSS:</b> PLL Analog Voltage for the core PLL
<b>System Management</b>		
SCL	I/O	SMBus Clock
SDA	I/O	SMBus Address/Data
SA[2:0]		DIMM Select ID
<b>Reset</b>		

**Table 29 — Pin Description (Continued)**

Signal	Type	Description
$\overline{\text{RESET}}$		Power Good Reset
<b>Miscellaneous Test</b>		
TEST (4 pins)	NC	Pin for debug and test. Must be floated on DIMM.
TESTLO (5 pins)	A	Pin for debug and test. Must be tied to Ground on DIMM
TESTLO_AB20	A	Pin for debug and test. Connected to two resistors. One resistor is connected to VCCFBD, the other resistor is connected to VSS.
TESTLO_AC20	A	Pin for debug and test. Connected to two resistors. One resistor is connected to VCCFBD, the other resistor is connected to VSS.
<b>Power Supplies</b>		
VCC (24 pins)	A	1.5V nominal supply for core IO
VCCFBD (8 pins)	A	1.5V nominal supply for FBD high speed IO
VDD (24 pins)	A	1.8V nominal supply for DDR IO
VSS (156 pins)	A	Ground
VDDSPD	A	3.3V nominal supply for SMB receivers and ESD diodes
<b>Other Pins</b>		
BFUNC	I	<b>Buffer Function Bit:</b> When BFUNC = 0, AMB is used as a regular buffer on FB-DIMM. When BFUNC = 1, AMB is used as either a repeater or a buffer for LAI function. On FB-DIMM, BFUNC is tied to Ground
RFU (18 pins)	NC	<b>Reserved for Future Use.</b> Must be floated on DIMM. RFU pins denoted by “a” are reserved for forwarded clocks in future AMB implementations.
<b>Other No Connect Pins</b>		
NC (129 pins)	NC	No Connect pins

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## 10 Reset

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### 10.1 Introduction

This chapter describes aspects of hardware reset specific to the Advanced Memory Buffer.

### 10.2 Platform Reset Functionality

The FBD channel provides a RESET# signal to initialize all AMBs on the channel. The generation of this signal is platform dependent, and may be asynchronous to the clock. The platform will assert RESET# at power up. This signal may be asserted at other times, such as a warm boot (i.e., a 3 key reset, or machine restart).

It is possible that platform conditions cause RESET# to be asserted at any time, including in the middle of DRAM commands. This could occur during a warm boot. Under these conditions, the Advanced Memory Buffer will be reset and the contents of memory are not guaranteed. The state of the DRAMs must be guaranteed when reinitialized for proper response (refer to 3.5.1 in Chapter 3 DDR Interface).

#### 10.2.1 Platform RESET# Requirements

RESET# must be asserted at power up, and may also be asserted at other times such as a warm boot.

- Asserting RESET# only at power up will allow error logging registers to be maintained through a warm boot cycle.
- Asserting RESET# at warm boot will clear all error logging registers.

There is no need to delay or lockout RESET# going to the FBD channel since the AMB will guarantee that the tDelay parameter is met. Reference Clocks must remain stable for at least 4 clock cycles after RESET# is asserted in order to allow the AMB to satisfy the tDelay requirement.

- RESET# must be asserted during power up, and for a minimum of 1mS after the FBD channel power and reference clocks SCK/ $\overline{\text{SCK}}$  are stable.
- RESET# must be asserted for a minimum of 100  $\mu\text{s}$ . This will only apply if RESET# is re-asserted while power and clocks remain stable.
- After initial power on, if the reference clock frequency is changed while RESET# is asserted, RESET# must not be deasserted until power and reference clocks SCK/ $\overline{\text{SCK}}$  have been stable for at least 1 ms.

#### 10.2.2 Advanced Memory Buffer RESET# Requirements

RESET# is asynchronously applied to all storage elements. Assertion of RESET# may or may not affect AMB PLL operation (depends on specific AMB PLL design).

Upon assertion of RESET#:

- DRAM CKE is driven low asynchronously with minimal delay (within 1 clock, asynch path from reset to CKE)
- DQ/DQS are don't care. C/A shall follow the pin state as listed in Section 3.3 for S3 mode, and in Section 10.2.3 for Power-up.
- DRAM CLK/ $\overline{\text{CLK}}$  continue to run with no short pulses generated within the tDelay period specified in JESD79-2A Table 36 (timing diagram in Figure 60).
- DRAM CLK/ $\overline{\text{CLK}}$  may be stopped after the tDelay has been satisfied.
- All internal register bits are set to their default values, including any error logging bits that are normally not reset by the channel reset.

### 10.2.2 Advanced Memory Buffer RESET# Requirements (cont'd)

- The initialization FSM is put into the disable state. All internal state machines are put in their default state.
- All southbound and northbound Tx outputs are put into electrical idle (EI) mode. All Tx outputs stay in EI mode until they are put into Training State (TS0) after deassertion of RESET#.

### 10.2.3 Power-Up and Suspend-to-RAM Considerations

In a suspend to RAM environment the DRAMs are put into self-refresh mode, and the FBD channel power may be removed. The DRAM power supply remains active. This supply is used by the AMB DRAM interface I/O circuits. The AMB must keep the CKE pins low, without glitches through this transition.

RESET# must be asserted before channel power goes away when entering S3.

During initial power-up, CKE and ODT will be driven low. Once all power supplies are on and stable, all the other command/address pins must be tri-stated to reduce current drawn from the V<sub>tt</sub> power supply (refer to section 3.3). CKE must be maintained low during this time without glitches to prevent the DRAMs from exiting self refresh mode. The RESET# signal will remain low during the power-up sequence, for at least 1mS after power and clocks are stable. CLK must be up and stable at the required frequency before CKE goes from low to high. The CKE signals must remain low until a command is received that takes the CKE signals high. This could be an exit self refresh command, or any of the DRAM CKE commands.

## 10.3 Reset Types

Types of reset:

- Hard resets occur when the RESET# signal is low. This usually occurs at power up.
- Fast resets occur when there is a reset event on the primary southbound FBD Link.
- SMBus resets affect only the SMBus interface.

## 10.4 Pads Controlling Reset

The Advanced Memory Buffer resets are controlled by the RESET# pad and the primary southbound FBD link pads. The RESET# pad resets the chip at power up. When the primary southbound FBD link pads indicate EI, a fast reset is started.

### 10.4.1 RESET# Pad

The RESET# pad is controlled by the platform until after power and  $SCK/\overline{SCK}$  are stable. RESET# asynchronously resets most of the chip to a safe initial state. As the chip comes out of reset, the Primary South FBD Link is expected to be in a reset state. As the link sequences through the first initialization sequence after power up, the Advanced Memory Buffer will not generate any DRAM commands other than to maintain CKE low and enable DRAM clocks at the appropriate time.

### 10.4.2 Primary FBD Link

When an EI occurs on the primary southbound FBD link a fast reset is started. This starts a handshake procedure putting the DRAMs into self-refresh mode and resetting the Advanced Memory Buffer. Fast reset does not reset the PLL and sticky registers.

## 10.5 Details

### 10.5.1 Cold Power-Up Reset Sequence

1. 1.5 V, 1.8 V, and 3.3 V power supplies comes up
  - RESET# asserted low while power supplies are coming up
  - CKE's are low upon 1.8 V power up
2. BIOS queries SPD on all the FBDs on the channel to determine operating conditions
  - channel frequency, compatible DIMMs, DRAM and AMB parameters
3. Clocks up and stable at required frequency
  - Reference Clocks should be stable for at least 1ms before RESET# deasserted
  - DRAM clocks ( $\text{CLK}/\overline{\text{CLK}}$ ) may be toggling at this time
4. RESET# deasserted high
  - CKE's to DRAMs remain low
5. No in-band or SMBus transactions for at least 2 ms after RESET# deasserted
6. AMB parameters critical for robust link initialization are programmed via SMBus
  - Architected link registers
    - LINKPARNXT: link frequency - Note: some AMBs may use this write to trigger PLL init  
After writing to LINKPARNXT, 200us is required prior to any in-band activity.  
Note: It is generally satisfied by additional SMBus activity.
    - FBDSBCFGNXT: SB transmitter drive strength, de-emphasis setting and pass-thru mode
    - FBDNBCFGNXT:NB transmitter drive strength, de-emphasis setting and pass-thru mode
  - Personality Bytes from SPD needed for link initialization
    - PERSBYTE[5:0]NXT:
    - remaining Personality bytes are not required for link init and may be loaded over the high speed FBD configuration register accesses
  - These “Next” register values must be transferred to the matching “Current” registers before the FBD link leaves the DISABLE state
    - Updates may be done right after the NXT register is updated when link is in electrical idle. Updates must be complete before the beginning of training.
7. FBD Link is initialized including CALIBRATION state.
8. Remaining AMB configuration is loaded over high speed FBD channel
  - CMD2DATA, remaining Personality bytes, other SPD parameters, DRAM parameters, Errors enabled, etc.
9. FBD Link goes through fast reset (no CALIBRATION) to establish the desired configuration
  - DRAM clocks should be stable at this time (i.e., after link train).
10. DRAM interface can now be established
  - a. MRS/EMRS setup using DCALCSR and DCALADDR
  - b. DRAM interface calibrated using DCALCSR
  - c. Optionally, Membist functionality can be used to test the DRAMs
  - d. DRAM's can be initialized using MemBist
  - e. AMB auto-refresh engine is enabled at this time.
11. Refresh must now be transferred to the host

### 10.5.1 Cold Power-Up Reset Sequence (cont'd)

- Option 1: Use fast reset on the link with DRAMs in self-refresh
  - clear DSREFTC:DISSREXIT to enable fast self refresh exit when link is re-established
  - put the link in disable state which automatically puts the DRAMs in self refresh.
  - Start the refresh engine on the host
  - bring up the link again
  - Host starts sending refresh commands as soon as L0 state reached
- Option 2: write control register to disable auto-refresh engine followed by
  - Clear DAREFTC:AREFEN to turn off auto-refresh
  - Host then immediately takes over sending refresh commands

12. Host now has complete control of the FBD Channel

## 10.6 Timing Diagrams

Timing diagrams will be released in a future revision of this document.

## 10.7 I/O Initialization

### 10.7.1 FBD Channel Initialization

Channel initialization states and uses of fast reset are described in the *FB-DIMM Architecture and Protocol Specification*.

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## 11 Registers

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This chapter defines the minimal subset of AMB configuration registers to support this version of the FBD protocol.

### 11.1 Access Mechanisms

The Advanced Memory Buffer (AMB) component supports PCI configuration space access as defined in the *PCI Local Bus Specification, Rev.2.2*. The internal registers of the AMB can be accessed in byte or double word (32-bit) quantities. All multi-byte numeric fields use “little-endian” ordering (i.e., lower addresses contain the least significant parts of the field). As a memory buffer (not a PCI device or bridge) the AMB is not fully compliant with this mechanism with respect to the standard registers (those with offsets 0-3Fh).

AMB will not be mapped into the host system's PCI Plug and Play hierarchy, but is accessed through a method that is host controller implementation specific.

Problems will occur if the host system maps the registers into the PCI PnP hierarchy.

Configuration accesses are transported on the FBD link as configuration read and write commands, which mimic the corresponding PCI commands.

#### 11.1.1 Conflict Resolution and Usage Model Limitations

AMB accepts configuration register reads and writes through the FBD link and through SMBus transactions. In Logic Analyzer Interface (LAI) mode, registers are not accessible through the in-band FBD link configuration read/write commands.

Registers do not incur read side-effects.

#### 11.1.2 FBD Data on Configuration Read Returns

FBD read return data from AMB is described in the *FB-DIMM Draft Specification: Architecture and Protocol*. Configuration reads are sent in northbound data frames. Only the bottom four bytes of this data are defined for a configuration access. The rest of the bytes in the read return are undefined. Legal CRCs are generated for these undefined inbound bytes.

#### 11.1.3 Non-Existent Register Bits

To comply with the PCI specification, accesses to non-existent registers and bits will be treated per Table 30:

**Table 30 — Access to “Non-existent” Register Bits**

Access to	Writes	Reads
<b>Registers in unimplemented functions</b>	Have no effect	AMB returns -1
<b>Registers not listed</b>	Have no effect	AMB returns all zeros
<b>Reserved bits in registers</b>	Software must read-modify-write to preserve the value	AMB returns implementation specific values



### 11.1.4 Register Attribute Definition

**Table 31 — Register Attributes Definitions**

Attribute	Abbreviation	Description
Read Only	RO	The bit is set by the hardware only and software can only read the bit. Writes to the register have no effect.
Read/Write	RW	The bit can be read or written by software.
Read/Write /Clear	RWC	The bit can be either read or cleared by software. In order to clear a bit, the software must write a one to it. Writing a zero to an RWC bit will have no effect. Hardware will set this bit.
Read/Write /Set	RWS	The bit can be either read or set by software. In order to set this RWS bit, the software must write a one to it. Writing a zero to an RWS bit will have no effect. Hardware will clear this bit.
Sticky	All of the above with “ST” appended to the end	The bit is “sticky” or unchanged by a link reset. These bits can only be defaulted by a power-up reset.
Reserved	RV	This bit is reserved for future expansion and must not be written. The <i>PCI Local Bus Specification</i> , Revision 2.2 requires that reserved bits must be preserved. Any software that modifies a register that contains a reserved bit is responsible for reading the register, modifying the desired bits, and writing back the result.

### 11.1.5 Binary Number Notation

When references are made to binary numbers, the following notation is used:

n'bXX

n - number of digits

b - indicates binary

XX - binary value

For example, 2'b01 is two binary digital of value “01”.

### 11.1.6 Function Mapping

The following functions are described in this chapter:

- 0) PCI Standard Header Identification Registers
- 1) FBD Link Registers
- 2) Implementation Specific FBD Registers
- 3) DDR and Miscellaneous Registers
- 4) Implementation Specific DDR Initialization and Calibration Registers
- 5) DFX Registers
- 6) IBIST, Bring-up and Debug Registers
- 7) Implementation Specific

### 11.1.6 Function Mapping (cont'd)

**Table 32 — Function Mapping Legend**

Fill	Description
RegName	Required Architected Register "RegName" in these bytes
Reserved	Reserved Register for future architecture in these bytes
RegName	Optional Architected Register "RegName" in these bytes <ul style="list-style-type: none"><li>No Implementation Specific Registers usage recommended</li></ul>
	Unused Register location available for Implementation Specific use

### 11.1.6 Function Mapping (cont'd)

**Table 33 — Function 0: PCI Standard Header Identification Registers**

DID	VID	00h	80h
		04h	84h
CCR	RID	08h	88h
HDR		0Ch	8Ch
		10h	90h
		14h	94h
		18h	98h
		1Ch	9Ch
		20h	A0h
		24h	A4h
		28h	A8h
RESERVED		2Ch	ACH
		30h	B0h
		34h	B4h
		38h	B8h
		3Ch	BCh
		40h	C0h
		44h	C4h
		48h	C8h
		4Ch	CCh
		50h	D0h
		54h	D4h
		58h	D8h
		5Ch	DCh
		60h	E0h
		64h	E4h
		68h	E8h
		6Ch	ECh
		70h	F0h
		74h	F4h
		78h	F8h
		7Ch	FCh

### 11.1.6 Function Mapping (cont'd)

**Table 34 — Function 1: FBD Link Registers**

RESERVED				00h	RESERVED				80h				
RESERVED				04h	RESERVED				84h				
RESERVED				08h	RESERVED			CBC	88h				
RESERVED				0Ch	EMASK				8Ch				
				10h	FERR				90h				
				14h	NERR				94h				
				18h	RESERVED		RECCFG		98h				
				1Ch	RECFBD1		RECFBD0		9Ch				
				20h	RECFBD3		RECFBD2		A0h				
				24h	RECFBD5		RECFBD4		A4h				
				28h	RECFBD7		RECFBD6		A8h				
				2Ch	RECFBD9		RECFBD8		ACH				
				30h	PERSBYTE3 NXT	PERSBYTE 2NXT	PERSBYTE 1NXT	PERSBYTE 0NXT	B0h				
				34h	PERSBYTE7 NXT	PERSBYTE 6NXT	PERSBYTE 5NXT	PERSBYTE 4NXT	B4h				
38h	PERSBYTE1 1NXT	PERSBYTE 10NXT	PERSBYTE 9NXT	PERSBYTE 8NXT	B8h								
3Ch	RESERVED		PERSBYTE 13NXT	PERSBYTE 12NXT	BCh								
40h	PERSBYTE3 CUR	PERSBYTE 2CUR	PERSBYTE 1CUR	PERSBYTE 0CUR	C0h								
44h	PERSBYTE7 CUR	PERSBYTE 6CUR	PERSBYTE 5CUR	PERSBYTE 4CUR	C4h								
48h	PERSBYTE1 1CUR	PERSBYTE 10CUR	PERSBYTE 9CUR	PERSBYTE 8CUR	C8h								
4Ch	RESERVED		PERSBYTE 13CUR	PERSBYTE 12CUR	CCh								
50h									D0h				
54h									D4h				
58h									D8h				
5Ch									DCh				
60h									E0h				
64h									E4h				
68h					C2DINCRCU R	C2DINCRN XT	CMD2DAT ACUR	CMD2DAT ANXT	E8h				
6Ch					RESERVED		C2DDECRC UR	C2DDECRC NXT	ECh				
70h													F0h
74h													F4h
78h									F8h				
7Ch									FCh				

### 11.1.6 Function Mapping (cont'd)

**Table 35 — Function 2: Implementation Specific FBD Registers**

RESERVED	00h	80h
RESERVED	04h	84h
RESERVED	08h	88h
RESERVED	0Ch	8Ch
	10h	90h
	14h	94h
	18h	98h
	1Ch	9Ch
	20h	A0h
	24h	A4h
	28h	A8h
	2Ch	ACh
	30h	B0h
	34h	B4h
	38h	B8h
	3Ch	BCh
	40h	C0h
	44h	C4h
	48h	C8h
	4Ch	CCh
	50h	D0h
	54h	D4h
	58h	D8h
	5Ch	DCh
	60h	E0h
	64h	E4h
	68h	E8h
	6Ch	ECh
	70h	F0h
	74h	F4h
	78h	F8h
	7Ch	FCh

### 11.1.6 Function Mapping (cont'd)

**Table 36 — Function 3: DDR and Miscellaneous Registers**

RESERVED	00h	UPDATED	TEMPHI	TEMPMID	TEMPLO	80h	
RESERVED	04h				TEMP	TEMPSTAT	84h
RESERVED	08h				88h		
RESERVED	0Ch				8Ch		
	10h				90h		
	14h	94h					
	18h	98h					
	1Ch	MB_START_ADDR				9Ch	
	20h	MB_END_ADDR				A0h	
	24h	MB_LFSR				A4h	
	28h	MBFADDRPTR				A8h	
	2Ch	RESERVED				ACh	
	30h	MB_ERR_DATA00				B0h	
	34h	MB_ERR_DATA01				B4h	
	38h	MB_ERR_DATA02				B8h	
	3Ch	MB_ERR_DATA03				BCh	
MBCSR	40h				MB_ERR_DATA04		C0h
MBADDR	44h				C4h		
MBDATA0	48h				C8h		
MBDATA1	4Ch				CCh		
MBDATA2	50h				D0h		
MBDATA3	54h				D4h		
MBDATA4	58h				D8h		
MBDATA5	5Ch				DCh		
MBDATA6	60h				E0h		
MBDATA7	64h				E4h		
MBDATA8	68h				E8h		
MBDATA9	6Ch				ECh		
DAREFTC					70h	F0h	
MTR	DSREFTC				74h	F4h	
DRT					78h	F8h	
DRC					7Ch	FCh	

## 11.1.6 Function Mapping (cont'd)

Table 37 — Function 4: Implementation Specific DDR Initialization and Calibration Registers

RESERVED	00h		80h
RESERVED	04h		84h
RESERVED	08h		88h
RESERVED	0Ch		8Ch
	10h		90h
	14h		94h
	18h		98h
	1Ch		9Ch
	20h		A0h
	24h	S3RESTORE0	A4h
	28h	S3RESTORE1	A8h
	2Ch	S3RESTORE2	ACH
	30h	S3RESTORE3	B0h
	34h	S3RESTORE4	B4h
	38h	S3RESTORE5	B8h
	3Ch	S3RESTORE6	BCh
DCALCSR	40h	S3RESTORE7	C0h
DCALADDR	44h	S3RESTORE8	C4h
	48h	S3RESTORE9	C8h
	4Ch	S3RESTORE10	CCh
	50h	S3RESTORE11	D0h
	54h	S3RESTORE12	D4h
	58h	S3RESTORE13	D8h
	5Ch	S3RESTORE14	DCh
	60h	S3RESTORE15	E0h
	64h		E4h
	68h		E8h
	6Ch		ECh
	70h		F0h
	74h		F4h
	78h		F8h
	7Ch	DDR2ODTC	FCh

### 11.1.6 Function Mapping (cont'd)

**Table 38 — Function 5: DFX Registers**

RESERVED		00h		TRANSCTRL	80h
RESERVED		04h		84h	
RESERVED		08h		88h	
RESERVED		0Ch		8Ch	
		10h		90h	
		14h		94h	
		18h		98h	
		1Ch		9Ch	
		20h		A0h	
		24h		A4h	
		28h		A8h	
		2Ch		ACh	
		30h		B0h	
		34h		B4h	
		38h		B8h	
TRANSCFG		3Ch	SBMATCHU	BCh	
TRANDERR1	TRANDERR0	40h	SBMATCHL0	C0h	
TRANDERR3	TRANDERR2	44h	SBMATCHL1	C4h	
TRANDERR5	TRANDERR4	48h	SBMATCHL2	C8h	
TRANDERR7	TRANDERR6	4Ch	SBMASKU	CCh	
	TRANDERR8	50h	SBMASKL0	D0h	
	54h	SBMASKL1	D4h		
	58h	SBMASKL2	D8h		
	5Ch		MMEVENTSEL	DCh	
	60h	EVENTSEL0		E0h	
	64h	EVENTSEL1		E4h	
	68h	EVENTSEL2		E8h	
	6Ch			ECh	
	70h	EVENT		F0h	
	74h	EVBUS		F4h	
	78h			F8h	
7Ch	STUCKL		EICNTL	FCh	



## 11.1.6 Function Mapping (cont'd)

Table 39 — Function 6: IBIST, Bring-up and Debug Registers

RESERVED	00h	SBFIBPORTCTL	80h
RESERVED	04h	SBFIBPGCTL	84h
RESERVED	08h	SBFIBPATTBUF1	88h
RESERVED	0Ch	SBFIBTXMSK	8Ch
	10h	SBFIBRXMSK	90h
	14h	SBFIBTXSHFT	94h
	18h	SBFIBRXSHFT	98h
	1Ch	SBFIBRXLNERR	9Ch
	20h	SBFIBPATTBUF2	A0h
	24h	SBFIBPATTBUF2EN	A4h
	28h		A8h
	2Ch		ACh
	30h	SBFIBINIT	B0h
	34h	SBIBISTMISC	B4h
	38h		B8h
	3Ch		BCh
	40h	NBFIBPORTCTL	C0h
	44h	NBFIBPGCTL	C4h
	48h	NBFIBPATTBUF1	C8h
	4Ch	NBFIBTXMSK	CCh
	50h	NBFIBRXMSK	D0h
	54h	NBFIBTXSHFT	D4h
	58h	NBFIBRXSHFT	D8h
	5Ch	NBFIBRXLNERR	DCh
	60h	NBFIBPATTBUF2	E0h
	64h	NBFIBPATTBUF2EN	E4h
	68h		E8h
	6Ch		ECh
	70h	NBFIBINIT	F0h
	74h	NBIBISTMISC	F4h
	78h		F8h
	7Ch		FCh

### 11.1.6 Function Mapping (cont'd)

**Table 40 — Functions 7: FBD DFX/Defeature Registers**

RESERVED	00h		80h
RESERVED	04h		84h
RESERVED	08h		88h
RESERVED	0Ch		8Ch
	10h		90h
	14h		94h
	18h		98h
	1Ch		9Ch
	20h		A0h
	24h		A4h
	28h		A8h
	2Ch		ACH
	30h		B0h
	34h		B4h
	38h		B8h
	3Ch		BCh
	40h		C0h
	44h		C4h
	48h		C8h
	4Ch		CCh
	50h		D0h
	54h		D4h
	58h		D8h
	5Ch		DCh
	60h		E0h
	64h		E4h
	68h		E8h
	6Ch		ECh
	70h		F0h
	74h		F4h
	78h		F8h
	7Ch		FCh

## 11.2 PCI Standard Header Identification Registers (Function 0)

### 11.2.1 VID: Vendor Identification Register

This register identifies the manufacturer of the AMB.

Function: 0 Offset:00h			
Bit	Attr	Default	Description
15:0	RO	VID	<b>Vendor Identification Number</b> Manufacturer's PCI ID number

### 11.2.2 DID: Device Identification Register

These registers combined with the vendor identification register uniquely identifies the AMB Devices.

Function: 0 Offset:02h			
Bit	Attr	Default	Description
15:0	RO	DID	<b>Device Identification Number</b> Identifies each function of the AMB

### 11.2.3 RID: Revision Identification Register

This register contains the revision number of the AMB.

Function:0 Offset:08h			
Bit	Attr	Default	Description
7:0	RO	RID	<b>Revision Identification Number: RID</b> Identifies this revision of AMB

### 11.2.4 CCR: Class Code Register

This register contains the Class Code for the AMB, specifying the device function.

Function: 0 Offset:09h			
Bit	Attr	Default	Description
23:1 6	RO	05h	<b>Base Class.</b> This field indicates the general device category. For the AMB, this field is hardwired to 05h, indicating it is a “memory controller”.
15:8	RO	00h	<b>Sub-Class.</b> This field qualifies the Base Class, providing a more detailed specification of the device function. For the AMB, this field is hardwired to 00h, indicating it is a “RAM”.
7:0	RO	00h	<b>Register-Level Programming Interface.</b> This field identifies a specific programming interface (if any), that device independent software can use to interact with the device. There are no such interfaces defined for “memory controllers”.

### 11.2.5 HDR: Header Type Register

This register identifies the header layout of the configuration space.

Function: 0 Offset:0Eh			
Bit	Attr	Default	Description
7	RO	1	<b>Multi-function Device.</b> Selects whether this is a multi-function device, that may have alternative configuration layouts. The AMB has more than the 256 bytes of configuration registers allotted to a single function. Therefore, the AMB is defined to be a multifunction device, and this bit is hardwired to 1.
6:0	RO	00h	<b>Configuration Layout.</b> This field identifies the format of the 10h through 3Fh space. The AMB uses header type “00”: these bits are hardwired to 00h.

## 11.3 FBD Link Registers (Function 1)

### 11.3.1 FBD Link Control and Status

#### 11.3.1.1 FBDS0: FBD Status 0

This register contains copies of status bits returned by the AMB in the most recent northbound status frame when SYNC command R[1:0] field is 2'b00.

**11.3.1.1 FBDS0: FBD Status 0 (cont'd)**

In the absence of SYNCs to this register, this register is not updated.

<b>Function:1 Offset:40h</b>			
<b>Bit</b>	<b>Attr</b>	<b>Default</b>	<b>Description</b>
7:5	RV	0h	Reserved
4	RO	0h	SP: Parity: This bit contains an odd parity bit that covers the S[3:0] field.
3	RO	0h	<b>S3: Northbound Debug Event</b> (1 = asserted, 0 = inactive): This bit is used to communicate debug events to the host.
2:1	RO	0h	<b>S[2:1]: Thermal Trip:</b> This field indicates various thermal conditions of the AMB as follows: <ul style="list-style-type: none"> <li>• 00 – Below TEMPLO</li> <li>• 01 – Above TEMPLO</li> <li>• 10 – Above TEMPMID and falling</li> <li>• 11 – Above TEMPMID and rising</li> </ul> The TEMPLO threshold is generally used to inform the host to accelerate refresh events. The TEMPMID threshold is generally used to inform the host that a thermal limit has been exceeded and that thermal throttling is needed. Refer to the RAS chapter for more details on thermal management.
0	RO	0h	S0: ERROR Asserted: This bit indicates an error has been detected by the AMB. Errors can be alert or other type.

**11.3.1.2 FBDS1: FBD Status 1**

This register contains copies of status bits returned by the AMB in the most recent northbound status frame when SYNC command R[1:0] field is 2'b01.

<b>Function:1 Offset:41h</b>			
<b>Bit</b>	<b>Attr</b>	<b>Default</b>	<b>Description</b>
7:5	RV	0h	Reserved
4	RO	0h	SP: Parity: This bit contains an odd parity bit that covers the S[3:0] field.
3:1	RV	0h	Reserved
0	RO	0h	S0: Data Merge Error: This bit indicates that the northbound data merge alignment logic of an intermediate AMB cannot met the timing required to merge its DRAM data into the northbound data stream when required. Refer to the initialization chapter for details.

**11.3.1.3 FBDS2: FBD Status 2**

This register contains copies of status bits returned by the AMB in the most recent northbound status frame when SYNC command R[1:0] field is 2'b10

Function:1 Offset:42h			
Bit	Attr	Default	Description
7:5	RV	0h	Reserved
4	RO	0h	SP: Parity: This bit contains an odd parity bit that covers the S[3:0] field.
3:0	RV	0h	Reserved

**11.3.1.4 FBDS3: FBD Status 3**

This register contains copies of bits that were returned by the AMB in the most recent northbound status frame when the SYNC command R[1:0] field is 2'b11. This can also be written with an override value that will be returned if selected during SYNC command.

Function:1 Offset:43h			
Bit	Attr	Default	Description
7:6	RV	0h	Reserved
5	RW	0h	OVREN: Use values written by user. Setting this bit causes the values specified in the lower 5 bits of this register returned as-is if requested by SYNC command.
4	RW	1h	USRPAR: User Specified parity for USRVAL
3:0	RW	0h	USRVAL: User Specified value

**11.3.1.5 MODES: Operating Mode**

This register contains overview configuration status of chip.

Function:1 Offset:5Ch			
Bit	Attr	Default	Description
7	RO	1	NORMAL: • 1 = Normal AMB Buffer
6	RO	0	LAI: • 1 = LAI
5	RO	0	REPEATER: • 1 = Repeater
4	RO	0	TRANSPARENT: • 1 = Transparent Test Mode
3:0	RV	0	Reserved

**11.3.1.6 FEATURES: Capabilities**

This register reports optional capabilities of this DIMM.

<b>Function:1 Offset:60h</b>			
<b>Bit</b>	<b>Attr</b>	<b>Default</b>	<b>Description</b>
31:15	RV	0h	Reserved
14:11	RO	Vendor Specific	DDRFREQ: DDR2 frequencies supported <ul style="list-style-type: none"> <li>• 1XXX = reserved</li> <li>• X1XX = DDR2-800</li> <li>• XX1X = DDR2-667</li> <li>• XXX1 = DDR2-533</li> </ul>
10	RO	Vendor Specific	VARLAT: Variable Read Latency Mode <ul style="list-style-type: none"> <li>• 1 = Support Variable Read Latency on data returns</li> <li>• 0 = Not supported</li> </ul>
9	RO	Vendor Specific	LAI: Logic Analyzer Interface Mode <ul style="list-style-type: none"> <li>• 1 = Support remapping DDR interface as Logic Analyzer Interface</li> <li>• 0 = Not supported</li> </ul>
8	RO	Vendor Specific	DMASK: Data Mask for non-ECC Write Data <ul style="list-style-type: none"> <li>• 1 = Support data mask with non-ECC Write</li> <li>• 0 = Not supported</li> </ul>
7	RO	Vendor Specific	LOS: Low Power Link State <ul style="list-style-type: none"> <li>• 1 = Support L0s state</li> <li>• 0 = Not supported</li> </ul>
6:2	RO	Vendor Specific	NBWC: Northbound Width Capability <ul style="list-style-type: none"> <li>• 1XXXX = 14 bits NB width supported</li> <li>• X1XXX = 14bits fail over to 13 bits mode supported.</li> <li>• XX1XX = 13 bits NB width supported</li> <li>• XXX1X = 13 bits fail over to 12 bits mode supported.</li> <li>•</li> </ul>
1:0	RO	Vendor Specific	SBWC: Southbound Width Capability <ul style="list-style-type: none"> <li>• X1 = 10 SB bits: Device supports 10-bits and 10-bit fail-over to 9-bits. Both configurations deliver 72-bits of data payload frame.</li> </ul> 1X = Reserved

**11.3.1.7 FBDLIS: FBD Link Initialization Status**

This register reports GB AMB FBD initialization status and is only valid when the link is up since it is not sticky.

<b>Function:1 Offset:64h</b>			
<b>Bit</b>	<b>Attr</b>	<b>Default</b>	<b>Description</b>
31:20	RV	0	Reserved
19	RO	0	DATAMERGEERROR: NorthBound Data Merge Error <ul style="list-style-type: none"> <li>1 = NB merge error</li> </ul>
18	ROST	0	<b>NBMERGEDIS: NorthBound Merge Disable</b> Set by TS2 packet addressed to it <ul style="list-style-type: none"> <li>1 = Disable NB merge</li> <li>Note: state in AMB should be sticky through fast link reset until new TS2 resets bit or hard pin reset</li> </ul>
17:12	RO	3Fh	NBWCFG: Northbound width configuration set by TS3 <ul style="list-style-type: none"> <li>See table in <i>FBD Channel Specification</i> for full decoding</li> <li>[5:4] = Selects 14, 13 or 12 lane operation.</li> <li>[3:0] - Selects none or one lane to map out</li> </ul>
11:8	RO	Fh	SBWCFG: Southbound width capability set by TS3 <ul style="list-style-type: none"> <li>See Table in <i>FBD Channel Specification</i> for full decoding</li> <li>[3:0] - Selects none or one lane to map out</li> </ul>
7	RV	0	Reserved
6	RO	0	<b>TS2RESP:</b> Responded to a TS2 packet addressed to it 1: TS2 was addressed to this AMB <ul style="list-style-type: none"> <li>In polling mode - DS matches TS2 AMB_ID value</li> <li>Undefined in other states</li> </ul>
5	RO	0	SB2NBLBMAP: Specifies if upper or lower SB lanes are reflected in TS1 Valid only during testing phase (TS1) 1 = upper SB bit lanes 0 = lower SB lanes
4	RO	0	LASTAMBFLAG: Indicates if this AMB is acting like the last AMB <ul style="list-style-type: none"> <li>In Disable, Calibrate - always 0.</li> <li>In training - Set if DS matches TS0 AMB_ID value</li> <li>Retains value after training till next reset.</li> </ul>
3:0	RO	0h	<b>LINITST: Link initialization state</b> Encoding is <ul style="list-style-type: none"> <li>0000 - Disable</li> <li>0001 - Calibrate</li> <li>0010 - Training</li> <li>0011 - Testing</li> <li>0100 - Polling</li> <li>0101 - Config</li> <li>0110 - L0</li> <li>0111 - L0s</li> <li>1000 - Recalibrate</li> </ul>



### 11.3.1.8 FBDSBCFGNXT: FBD SB Link Electrical Configuration

This register contains next settings of control bits to set link electrical parameters to match link length and frequency characteristics.

**Note:** The Margin Drive Strength settings are not to be used during normal function mode, and therefore do not have a corresponding CUR register. New margin settings only take effect after the channel comes out of fast reset (channel Electrical Idle). Transmitters are not required to dynamically adjust drive strengths on the fly. Desired voltage margin settings are loaded into FBDSBCFGNXT, function 1, offsets 54h when SBTXDRVMAR is HIGH, and SB transmitters will be driven accordingly.

<b>Function:1 Offset:54h</b>			
<b>Bit</b>	<b>Attr</b>	<b>Default</b>	<b>Description</b>
7:6	RV	0h	Reserved
5	RWST	0h	<b>SBTXDRVMAR: SB TRANSMIT MARGIN</b> '1' = margin drive strength '0' (default) = no change to normal drive strength
4:3	RWST	00b	<b>SBTXDRVCUR: SB TRANSMIT DRIVE STRENGTH</b> Normal drive strengths: (SBTXDRVMAR == 0) '11' = Small '10' = reserved '01' = Regular '00' = Large <b>SBTXDRVCUR:</b> Margin test drive strengths: (SBTXDRVMAR == 1) '11' = 160 mv minimum '10' = 250 mv minimum '01' = 340 mv minimum '00' = 430 mv minimum
2:1	RWST	10b	<b>SBTXDEEMP:</b> 00 = 0 dB 01 = 3.5 dB 10 = 6 dB 11 = 9.5 dB
0	RWST	1b	<b>SBRESYNCEN:</b> '1' = SB pass-thru data is in Re-sync mode '0' = SB pass-thru is in Re-sample mode.

**11.3.1.8 FBDS0: FBD Status 0 (cont'd)****Optional feature “Timing Margin Test”**

Receivers are not required to dynamically adjust error offset on the fly. New margin settings only take effect after the channel comes out of fast reset. Receivers are not required to dynamically adjust timing margin on the fly. Desired timing margin settings are loaded into FBDSBCFGNXT and FBDNBCFGNXT, function 1, offsets 5Ah and 5Bh. Refer to FB-DIMM Design for Test, Design for Validation (DFx) Specification v1.0 section 7.3 for details.

Function:1 Offset:5Ah			
Bit	Attr	Default	Description
7	RWST	0h	<b>SBRXMARPOL: SOUTHBOUND RECEIVER TIMING MARGIN POLARITY</b> Sets the southbound receiver margin error polarity 0 = early 1 = late
6:0	RWST	0h	<b>SBRXMAROFF: SOUTHBOUND RECEIVER TIMING MARGIN OFFSET</b> This field sets the magnitude of the timing sampling error applied to the SB receiver. A minimum implementation requires 6:4 to be implemented. Specific implementations may choose to implement additional error offset granularity using some or all of bits 3:0. ‘111111’ = full error ‘000000’ = zero error all other values will provide binary monotonic error insertion between zero and full sampling error

### 11.3.1.9 FBDNBCFGNXT: FBD NB Link Electrical Configuration

This register contains next settings of control bits to set link electrical parameters to match link length and frequency characteristics.

**Note:** The Margin Drive Strength settings are not to be used during normal function mode, and therefore do not have a corresponding CUR register. New margin settings only take effect after the channel comes out of fast reset (channel Electrical Idle). Transmitters are not required to dynamically adjust drive strengths on the fly. Desired voltage margin settings are loaded into FBDNBCFGNXT, function 1, offsets 55h when NBTXDRVMAR is HIGH, and NB transmitters will be driven accordingly

Function:1 Offset:55h			
Bit	Attr	Default	Description
7:6	RV	0h	Reserved
5	RWST	0h	<b>NBTXDRVMAR: NB TRANSMIT MARGIN</b> '1' = margin drive strength '0' (default) = no change to normal drive strength
4:3	RWST	00b	<b>NBTXDRVCUR: NB TRANSMIT DRIVE STRENGTH</b> Normal drive strengths: (NBTXDRVMAR == 0) '11' = Small '10' = reserved '01' = Regular '00' = Large <b>NBTXDRVCUR:</b> Margin test drive strengths: (NBTXDRVMAR == 1) '11' = 160 mv minimum '10' = 250 mv minimum '01' = 340 mv minimum '00' = 430 mv minimum
2:1	RWST	10b	<b>NBTXDEEMP:</b> 00 = 0 dB 01 = 3.5dB 10 = 6dB 11 = 9.5dB
0	RWST	1b	<b>NBRESYNCEN:</b> '1' = NB pass-thru data is in Re-sync mode '0' = NB pass-thru is in Re-sample mode.

**11.3.1.9 FBDNBCFGNXT: FBD NB Link Electrical Configuration (cont'd)****Optional feature “Timing Margin Test”**

Receivers are not required to dynamically adjust error offset on the fly. New margin settings only take effect after the channel comes out of fast reset. Receivers are not required to dynamically adjust timing margin on the fly. Desired timing margin settings are loaded into FBDSBCFGNXT and FBDNBCFGNXT, function 1, offsets 5Ah and 5Bh. Refer to FB-DIMM Design for Test, Design for Validation (DFx) Specification v1.0 section 7.3 for details.

<b>Function:1 Offset:5Bh</b>			
<b>Bit</b>	<b>Attr</b>	<b>Default</b>	<b>Description</b>
7	RWST	0h	<b>NBRXMARPOL: NORTHBOUND RECEIVER TIMING MARGIN POLARITY</b> Sets the northbound receiver margin error polarity 0 = early 1 = late
6:0	RWST	0h	<b>NBRXMAROFF: NORTHBOUND RECEIVER TIMING MARGIN OFFSET</b> This field sets the magnitude of the timing sampling error applied to the NB receiver. A minimum implementation requires 6:4 to be implemented. Specific implementations may choose to implement additional error offset granularity using some or all of bits 3:0. ‘111111’ = full error ‘000000’ = zero error all other values will provide binary monotonic error insertion between zero and full sampling error

**11.3.1.10 LINKPARNXT: FBD Link Frequency**

This register contains current settings of control bits to set link electrical parameters to match link length and frequency characteristics.

<b>Function:1 Offset:56h</b>			
<b>Bit</b>	<b>Attr</b>	<b>Default</b>	<b>Description</b>
15:2	RV	0h	Reserved
1:0	RWST	00b	<b>CFREQ: Current Link Frequency</b> <ul style="list-style-type: none"> <li>• 11 = DDR2-800</li> <li>• 10 = DDR2-667</li> <li>• 01 = DDR2-533</li> <li>• 00 = Uninitialized</li> </ul>

**11.3.1.11 FBDSBCFGCUR: FBD SB Link Electrical Configuration**

This register contains current settings of control bits to set link electrical parameters to match link length and frequency characteristics.

<b>Function:1</b> <b>Offset:50h</b>			
Bit	Attr	Default	Description
7:5	RV	0h	Reserved
4:3	ROST	00b	<b>SBTXDRVCUR:</b> '11' = Small '10' = reserved '01' = Regular '00' = Large
2:1	ROST	10b	<b>SBTXDEEMP:</b> 00 = 0 dB 01 = 3.5dB 10 = 6dB 11 = 9.5dB
0	ROST	1	<b>SBRESYNCEN:</b> '1' = SB pass-thru data is in Re-sync mode '0' = SB pass-thru is in Re-sample mode.

**11.3.1.12 FBDNBCFGCUR: FBD NB Link Electrical Configuration**

This register contains current settings of control bits to set link electrical parameters to match link length and frequency characteristics.

<b>Function:1 Offset:51h</b>			
<b>Bit</b>	<b>Attr</b>	<b>Default</b>	<b>Description</b>
7:5	RV	0h	Reserved
4:3	ROST	00	<b>NBTXDRVCUR:</b> '11' = Small '10' = reserved '01' = Regular '00' = Large
2:1	ROST	10b	<b>NBTXDEEMP:</b> 00 = 0 dB 01 = 3.5dB 10 = 6dB 11 = 9.5dB
0	ROST	1	<b>NBRESYNCEN:</b> '1' = NB pass-thru data is in Re-sync mode '0' = NB pass-thru is in Re-sample mode.

**11.3.1.13 LINKPARCUR: FBD Link Frequency**

This register contains current settings of control bits to set link electrical parameters to match link length and frequency characteristics

<b>Function:1 Offset:52h</b>			
<b>Bit</b>	<b>Attr</b>	<b>Default</b>	<b>Description</b>
15:2	RV	0h	Reserved
1:0	ROST	01	CFREQ: Current Link Frequency <ul style="list-style-type: none"> <li>• 11 = DDR2-800</li> <li>• 10 = DDR2-667</li> <li>• 01 = DDR2-533</li> <li>• 00 = Reserved</li> </ul>

**11.3.1.14 FBDLOCKTO: FBD Bit Lock Time Out Register**

This register contains.

<b>Function:1</b> <b>Offset:68h</b>			
<b>Bit</b>	<b>Attr</b>	<b>Default</b>	<b>Description</b>
15:2	RWST	0594h	BLTOCNT: Bit Lock Time Out Counter default: 1428 frames
1:0	RWST	0h	NBLINKCFG: Norht bound Link Config 00 = 14 lane 01 = 13 lane 10 = 12 lane 11 = reserved

**11.3.1.15 FBDHAC: FBD Hot Add Control**

This register contains control to aid in hot add functionality.

<b>Function:1</b> <b>Offset:6Ch</b>			
<b>Bit</b>	<b>Attr</b>	<b>Default</b>	<b>Description</b>
7:2	RV	0	Reserved
1	RO	0	NB_DATA_ALL_ONES_FLAG: <ul style="list-style-type: none"> <li>1 = Receiving ones on sufficient NB lanes to support init</li> <li>0 = Not receiving calibrate handshake on NB Rx</li> </ul>
0	RW	0	DRIVE_ONES_SB: <ul style="list-style-type: none"> <li>1 = Enable SB Tx Outputs and drive one's</li> <li>0 = Normal operation</li> </ul>

**11.3.1.16 RECALDUR: FBD Recalibrate Duration**

This register determines the duration of the Recalibration state between 32 and 42 frames. During recalibration state all commands and CRC are ignored.

Function:1 Offset:70h			
Bit	Attr	Default	Description
7	RV	0	Reserved
6:1	RW	0h	Recalibrate_Duration: This field sets the duration of the Recalibrate state once a sync command with the ERC bit. set is received. Legal values are between 32 and 42. Functionality if set outside this range is undefined. <ul style="list-style-type: none"> <li>• &gt; '42d (101010b) = undefined</li> <li>• = '42d (101010b) = ignore for 42 frames after Sync</li> <li>• ....</li> <li>• = 32d (100000b) = ignore for 32 frames after Sync</li> <li>• &lt;32d (100000b) = undefined</li> </ul>
0	RV	0	Reserved

**11.3.1.17 L0SDUR: FBD L0S State Duration**

This register determines the duration of the L0s state between 32 and 42 frames.

Function:1 Offset:74h			
Bit	Attr	Default	Description
7	RV	0	Reserved
6:1	RW	0h	L0s_Duration: This field sets the duration of the L0s state once a sync command with the EL0s bit. set is received. Legal values are between 32 and 42. Functionality if set outside this range is undefined. <ul style="list-style-type: none"> <li>• &gt; '42d (101010b) = undefined</li> <li>• = '42d (101010b) = ignore for 42 frames after Sync</li> <li>• ....</li> <li>• = 32d (100000b) = ignore for 32 frames after Sync</li> <li>• &lt;32d (100000b) = undefined</li> </ul>
0	RW	0b	L0s_Enable: When 1 L0s mode is enabled



**11.3.1.18 SYNCTRAININT: SYNC Train Interval Register**

This register sets the typical spacing of sync commands on the link.

Function:1 Offset:78h			
Bit	Attr	Default	Description
7:0	RWST	2Ah	SyncTrainInt: This field sets the min spacing for sync cmds default value 42d (101010b) min value 32, max value=255

**11.3.1.19 SBCALSTATUS: Southbound Calibration Status**

This register contains the pass/fail information of the last calibration on a per lane basis for the southbound. The AMB is expected to log the information when it is asked to go through calibration. The register is always cleared when entering the calibration state. This register will be used for debug purposes.

Function:1 Offset:7Ch			
Bit	Attr	Default	Description
15:10	RV	0h	Reserved
9:0	RWST	0h	CALSTATUS: Calibration status 0 - Pass 1 - Fail <b>Note:</b> Read/Write for firmware debug purposes ONLY

**11.3.1.20 NBCALSTATUS: Northbound Calibration Status**

This register contains the pass/fail information of the last calibration on a per lane basis for the southbound. The AMB is expected to log the information when it is asked to go through calibration. The register is always cleared when entering the calibration state. This register will be used for debug purposes.

Function:1 Offset:7Eh			
Bit	Attr	Default	Description
15:14	RV	0h	Reserved
13:0	RWST	0h	CALSTATUS: Calibration status 0 - Pass 1 - Fail <b>Note:</b> Read/Write for firmware debug purposes ONLY

### 11.3.2 Error Registers

#### 11.3.2.1 EMASK: Error Mask

This register masks errors in the FERR and NERR registers as well as disabling some types of error detection. A ‘0’ in any field enables that error. A ‘1’ in any field masks (disables) that error. Multiple bits can be set in this register. An enabled error sets error status, updates error logs, and generates link signals. A masked error does not affect error status, error logs, or link signals.

<b>Function:1 Offset:8Ch</b>			
<b>Bit</b>	<b>Attr</b>	<b>Default</b>	<b>Description</b>
31:6	RV	0	Reserved
5	RWST	1	INJERR: Error Injection has sourced an injected error bit in the status return field (optional)
4	RWST	1	INJALERT: Error Injection has sourced an injected alert error (optional)
3	RWST	0	FEWEDGES: tClk Training Violation (no sync cmd for 2x SYNCTRAININT - typically 84 frames)
2	RWST	1	OVERTEMP: Temp > TEMPHI and temp enabled
1	RWST	1	UNIMPLCFG: Unimplemented Configuration Address
0	RWST	0	CMDCRCERR: SB CRC Error

#### 11.3.2.2 FERR: First Error

This register contains bits specifying which errors occurred first as related to the FBD channel.

<b>Function:1 Offset:90h</b>			
<b>Bit</b>	<b>Attr</b>	<b>Default</b>	<b>Description</b>
31:6	RV	0	Reserved
5	RWCST	0	INJERR: Error Injection has sourced an injected error bit in the status return field (optional)
4	RWCST	0	INJALERT: Error Injection has sourced an injected alert error (optional)
3	RWCST	0	FEWEDGES: tClk Training Violation (no sync cmd for 2x SYNCTRAININT - typically 84 frames) Logs in RECFBD registers. Sends Alerts NB. Triggers auto self refresh SM. .
2	RWCST	0	OVERTEMP: Temp > TEMPHI and temp enabled Fatal. AMB shuts down.
1	RWCST	0	UNIMPLCFG: Unimplemented Configuration Address Correctable. Logs in RECCFG* registers. AMB drops the command.
0	RWCST	0	CMDCRCERR: SB CRC Error Correctable. Logs in RECFBD registers. AMB drops the current command and sources alerts

### 11.3.2.3 NERR: Successive Error

This register is used to report successive errors. More than two bits can be set in this register. This register contains bits specifying which errors occurred as related to the FBD channel.

A first error may also cause a successive error to be logged in the NERR.

Function:1 Offset:94h			
Bit	Attr	Default	Description
31:6	RV	0	Reserved
5	RWCST	0	INJERR: Error Injection has sourced an injected error bit in the status return field (optional)
4	RWCST	0	INJALERT: Error Injection has sourced an injected alert error (optional)
3	RWCST	0	FEWEDGES: tClkTraining Violation (no sync cmd for 2x SYNCTRAININT - typically 84 frames) Logs in RECFBD registers. Sends Alerts NB. Triggers auto self refresh SM.
2	RWCST	0	OVERTEMP: Temp > TEMPHI and temp enabled Fatal. AMB shuts down.
1	RWCST	0	UNIMPLCFG: Unimplemented Configuration Address Correctable. Logs in RECCFG* registers. Drops the command.
0	RWCST	0	CMDCRCERR: SB CRC Error Correctable. Logs in RECFBD registers. Drops the current command and sources alerts.

### 11.3.2.4 RECCFG: Configuration Register Error Log

This register contains the received address for an unimplemented configuration register access error. The contents of this register are only valid when the error that set this register is logged in the FERR or NERR register.

Function:1 Offset:98h			
Bit	Attr	Default	Description
15:13	RV	0	Reserved
12:10	RWST	0h	function: <b>Note:</b> Read/Write for firmware debug purposes ONLY
9:8	RWST	0h	size: 00 = one byte 01 = two bytes 10 = three bytes 11 = four bytes <b>Note:</b> Read/Write for firmware debug purposes ONLY
7:0	RWST	0h	register address: <b>Note:</b> Read/Write for firmware debug purposes ONLY

### 11.3.2.5 RECFBD[9:0]: FBD Error Log

.This register contains FBD frame data received that matches the logged frame error.

Captures {BC} from frame N and A from frame N+1 where

[11:8] = A[n+1]

[7:4] = C[n] slot

[3:0] = B[n] slot

The contents of this register are only valid when one of the errors that set this register is logged in the FERR register. The contents of this register should not change until the error indication is cleared from the FERR register.

<b>Function:1</b> <b>Offset:AEh, ACh, AAh, A8h, A6h, A4h, A2h, A0h, 9Eh, 9Ch</b>			
Bit	Attr	Default	Description
15:12	RV	0	Reserved
11:0	RWST	0	FRMDATA: Frame data for lane n <b>Note:</b> Read/Write for firmware debug purposes ONLY

### 11.3.3 PERSONALITY BYTES Loaded from the SPD

These bytes allow for AMB implementation specific settings to be loaded in an architected way by BIOS without BIOS being aware of specific AMB requirements. Each AMB vendor defines how these bytes should be loaded for the specific DIMM being built. The values to be loaded into these bytes are stored in the SPD EEPROM on the DIMM.

The first six bytes are required to be loaded into the AMB via SMBus before link initialization to allow for configuration information needed for robust link operation.

The remaining 8 bytes must be loaded before the FBD begins normal operation.

Usage of these bytes can include

- DDR electrical parameters to optimize performance on a given DIMM
  - e.g., DLL delay settings, various IO driver slew settings
- Enable/disable of various optimizations that may have been included in the design but can be turned off if they are not needed on this DIMM or they have unanticipated side effects - e.g., power save modes, alternate clock recovery algorithms
- Temperature Sensor offsets
- Internal clock domain phase offsets

**11.3.3.1 PERSBYTE[13:0]NXT: Personality Bytes**

<b>Function:1</b> <b>Offset:BDh:B0h</b>			
Bit	Attr	Default	Description
7:0	RWST	0	PData: Personality Data Byte Implementation specific registers

**11.3.3.2 PERSBYTE[13:0]CUR: Personality Bytes**

<b>Function:1</b> <b>Offset:BDh:B0h</b>			
Bit	Attr	Default	Description
7:0	ROST	0	PData: Personality Data Byte Implementation specific registers

**11.3.4 Advanced Memory Buffer Hardware Configuration Registers****11.3.4.1 CMD2DATANXT: Next Value of Command to Data Delay**

This register has the next value of the command to data delay. This will be used after the next fast reset. Value comes from SPD.

<b>Function:1</b> <b>Offset:E8h</b>			
Bit	Attr	Default	Description
7:4	RWST	0h	<b>DLYFRMS: Number of frames</b> This specifies full frame delay part of the command to data delay. 0 - 9: Valid delays 10 - 15: Reserved
3:0	RWST	0h	<b>DLYFRAC: Fractional delay of command to data</b> This specifies fractional frame delay part of the command to data delay. 0 - 11: Specifies the delay in 1UI increments 12 - 15: Reserved

**11.3.4.2 CMD2DATACUR: Current Value of Command to Data Delay**

This register has the current value of the command to data delay.

Function:1 Offset:E9h			
Bit	Attr	Default	Description
7:4	ROST	0h	<b>DLYFRMS: Number of frames</b> This specifies full frame delay part of the command to data delay. 0 - 9: Valid delays 10 - 15: Reserved
3:0	ROST	0h	<b>DLYFRAC: Fractional delay of command to data</b> This specifies fractional frame delay part of the command to data delay. 0 - 11: Specifies the delay in 1UI increments 12 - 15: Reserved

**11.3.4.3 C2DINCRNXT: Next Value of Command to Data Delay Increment**

This register has the next value of the command to data incremental delay. This will be used after the next fast reset. This will be used by the last AMB to delay driving the data beyond that specified in the command to data delay.

Function:1 Offset:EAh			
Bit	Attr	Default	Description
7:2	RV	0h	Reserved
1:0	RWST	0h	<b>INCRDLY: Incremental Delay for command to data</b> 0 - 3: Specifies the incremental delay in frames

**11.3.4.4 C2DINRCUR: Current Value of Command to Data Delay Increment**

This register has the current value of the command to data incremental delay. This will be used by the last AMB to delay driving the data beyond that specified in

Function:1 Offset:EBh			
Bit	Attr	Default	Description
7:2	RV	0h	Reserved
1:0	ROST	0h	<b>INCRDLY: Incremental Delay for command to data</b> 0 - 3: Specifies the incremental delay in frames

#### 11.3.4.5 C2DDECRNXT: Next Value of Command to Data Delay Decrement

This register has the next value of the command to data decrement delay. This will be used after the next fast reset. This will only be used by AMBs supporting Variable Read Delay.

Function:1 Offset: ECh			
Bit	Attr	Default	Description
7:4	RV	0h	Reserved
3:0	RWST	0h	<b>DECFRMS: Number of frames</b> This specifies full frame decrease in the command to data delay of this DIMM. 0- 15: number of frames

#### 11.3.4.6 C2DDECRCUR: Current Value of Command to Data Delay Decrement

This register has the current value of the command to data decrement delay. This is only valid on AMBs supporting Variable Read Delay.

Function:1 Offset: EDh			
Bit	Attr	Default	Description
7:4	RV	0h	Reserved
3:0	ROST	0h	<b>DECFRMS: Number of frames</b> This specifies full frame decrease in the command to data delay of this DIMM. 0- 15: number of frames

### 11.4 Implementation Specific FBD Registers (Function 2)

These registers are implementation specific.

### 11.5 DDR and Miscellaneous Registers (Function 3)

#### 11.5.1 Memory BIST Registers

**11.5.1.1 MBCSR: MemBIST Control**

Architected MemBIST control interface.

**MemBIST Control Table**

Function:3 Offset:40h			
Bit	Attr	Default	Description
31	RWS	0	START: Start operation: 1 => Set this bit to begin MemBIST execution. 0 => Hardware will clear this bit when MemBIST execution is completed.
30	RW	0	PF: Fail/Pass indicator: Write to 0 when start MemBIST. Hardware will set to 1 when a failure is detected. 0 => Pass 1 => Fail <b>Note:</b> Read/Write for firmware debug purposes ONLY
29	RW	0	HALT: Halt on Error 0 => Operation will not halt due to a detected error. 1 => Operation will halt after read-compare data error is detected.  MemBIST will complete the current transaction before halting. This may result in multiple errors being logged.
28	RW	0	ABORT: Membist test abort. When test abort bit is set, MBCSR bit 31 (Start operation, RWS) needs to be set to "0" at the same time to avoid restarting MemBIST. 0 => Normal operation. 1 => Need to abort the test during Membist operation.  If there is any following membist test after the abort test, bit [28] needs to be cleared.  The Write to set MBCSR.abort must occure at least tRFC after the Write to set MBCSR.start. Otherwise subsequent MemBIST operations may fail. tRFC value is set in DAREFTC.trfc (Function3, offset70h, bit field 23:16).
27	RW	0	SPARE:



**MemBIST Control Table (Continued)**

<b>Function:3 Offset:40h</b>			
<b>Bit</b>	<b>Attr</b>	<b>Default</b>	<b>Description</b>
26:24	RW	000	<p>ALGO: Embedded Algorithm selection:</p> <p>When Embedded algorithm is applied, please program the following bits at the same time.</p> <ul style="list-style-type: none"> <li>I/ Select bit[5:4] for the initial command execution mode.</li> </ul> <p>Except for the Data Retention stepII for selecting "10: read only with data comparison", program "01: write only without data comparison" for the rest of algorithms.</p> <ul style="list-style-type: none"> <li>II/ Program MBCSR bit[11:10] to select FastX, FastY, FastXY</li> <li>III/Program proper start/end address registers and correspondent MTR value for DIMM type.Do not leave start and end address register as default "00" or the same value. Algorithm did not support single address mode.</li> <li>IV/ Program MBCSR bit 14 to select failure address logger or failure bits location accumulator.</li> </ul> <p>Embedded Algorithm selection:</p> <p>000 =&gt; No embedded algorithm is selected. Normal command will be executed from the selection of MBCSR bits field [5:4]</p> <p>001 =&gt; Scan: ^ (WD1); ^ (RD2); ^ (WI3); ^ (RI4)</p> <p>010 =&gt; Undefined</p> <p>011 =&gt; Data Retention Write or Init: ^ (WD1);</p> <p>100 =&gt; Data Retention Read : ^ (RD2);</p> <p>101 =&gt; Mats +: ^ (WD1); ^ (RD2, WI3); v (RI4, WD5);</p> <p>110 =&gt; March C-: ^ (WD1); ^ (RD2, WI3); ^ (RI4, WD5); v (RD6, WI7); v (RI8, WD9); v (RD10);</p> <p>111 =&gt; Undefined</p>
23:22	RV	00	Reserved
21:20	RW	00	<p>CS: CS[1:0] selection in MemBIST mode</p> <p>01: select Rank 0</p> <p>10: select Rank 1</p> <p>00: Reserved</p> <p>11: Reserved</p>
19	RW	0	INVERT: Invert data pattern when data is written out to DRAM.
18:16	RW	000	<p>FIXED: Fixed data pattern selection for MemBIST operation</p> <p>000 =&gt; 0</p> <p>001 =&gt; F</p> <p>010 =&gt; A</p> <p>011 =&gt; 5</p> <p>100 =&gt; C</p> <p>101 =&gt; 3</p> <p>110 =&gt; 9</p> <p>111 =&gt; 6</p>

**MemBIST Control Table (Continued)**

<b>Function:3 Offset:40h</b>			
<b>Bit</b>	<b>Attr</b>	<b>Default</b>	<b>Description</b>
15	RW	0	<p>ENABLE288: Enable 288 bits user defined pattern for memory fill write only. There is no data comparison, error logger functions for 288 bits user defined data.</p> <p>0 =&gt; 144 bits user defined data pattern when MBCSR[9:8] selects user defined data.</p> <p>1 =&gt; 288 bits user defined data pattern when MBCSR[9:8] selects user defined data.</p>
14	RW	0	<p>MBDATA: Selects use of MBDATA for error log field for LFSR, Circular Shift and user defined data modes. This field has no effect on fixed data patterns.</p> <p>0 =&gt; use MBDATA0/1/2/3/8 for failure data bit location accumulator.</p> <p>1 =&gt; use MBDATA0/1/2/3/8 to log 5 failure addresses .</p>
13	RW	0	<p>ABAR: MemBIST output address compliment for FastX, FastY, and FastXY. Whenever this bit is enabled, Bank, Row, Column address will be inverted on alternate addresses as described in the MemBIST chapter.</p> <p>0 =&gt; Regular addressing</p> <p>1 =&gt; Dynamic address inversion (see more description in MemBIST Chapt).</p>
12	RW	0	<p>ADIR: Address decode direction for FastX, Fast Y, FastXY</p> <p>0 =&gt; Address increments</p> <p>1 =&gt; Address decrements</p>
11:10	RW	00	<p>FAST: Address sequencing</p> <p>00 =&gt; addressing with XZY toggling (column-&gt;bank-&gt;row)</p> <p>01 =&gt; Fast Y with fixed bank</p> <p>10 =&gt; Fast X with fixed bank</p> <p>11 =&gt; Fast XY with fixed bank</p>
9:8	RW	00	<p>DTYPE: Data type selection:</p> <p>00 =&gt; Fixed data pattern, selected by MBCSR bits 18:16</p> <p>01 =&gt; 144 or 288 bits user defined data</p> <p>10 =&gt; Circular shift data</p> <p>11 =&gt; LFSR data, seeded from 32 bit LFSR seed register.</p> <p>Circular shift data and LFSR data type should not be used for single address operation (ATYPE = 01).</p>

**MemBIST Control Table (Continued)**

<b>Function:3 Offset:40h</b>			
<b>Bit</b>	<b>Attr</b>	<b>Default</b>	<b>Description</b>
7:6	RW	00	ATYPE: Address type 00 => Reserved 01 => Single physical address operation, contained in MBADDR row/column/bank. 10 => start/end physical address range defined in MB_START_ADDR & MB_END_ADDR registers. <ul style="list-style-type: none"> <li>In FastX, FastY and FastXY modes, only the bank specified in MB_START_ADDR will be exercised.</li> </ul> 11 => full address range of the DIMM as defined in MTR register which specifies the number of banks, rows, and columns. <ul style="list-style-type: none"> <li>In FastX, FastY and FastXY modes, only the bank 0 will be exercised.</li> </ul> Full address test supports XZY addressing (column->bank->row) and fastX/fastY/fastXY .
5:4	RW	00	CMD: Command execution: 00 => Read only without data comparison 01 => Write only without data comparison 10 => Read with data comparison 11 => Write followed by Read with data comparison
3:0	RV	0	Reserved

**11.5.1.2 MBADDR: Memory Test Address**

The register is used by MemBIST only when testing to a single memory location.

(MBCSR.atype = 2b'01)

<b>Function:3 Offset:44h</b>			
<b>Bit</b>	<b>Attr</b>	<b>Default</b>	<b>Description</b>
31:16	RWST	0000h	ROW: Row Address 15:0
15	RWST	0	SPARE:
14:3	RWST	0000h	COL: Column Address BL8[14:3] <==> DRAM Column Address 15:11,9:3 BL4[14:3] <==> DRAM Column Address 14:11,9:2
2:0	RWST	000	BA: Bank Address 2:0

**11.5.1.3 MBDATA[9:0]: Memory Test Data**

<b>Function:3</b> <b>Offset:6Ch, 68h, 64h, 60h,5Ch, 58h, 54h, 50h,4Ch, 48h</b>			
<b>Bit</b>	<b>Attr</b>	<b>Default</b>	<b>Description</b>
31:0	RWST	0000h	DATA: see functional description below for definition by mode and register

## 11.5.1.3 MBDATA[9:0]: Memory Test Data (cont'd)

Table 41 — Functional Mapping of MemBIST Data Fields by Test Mode

Reg	Bit	Offset	Description by mode (note: MBCSR.dtype, MBCSR.mbddata and MBCSR.enable288 select mode)				
			Fixed Data Pattern	144 bit User Defined Pattern	Circular Shift	LFSR	288 bit User defined pattern
MBDATA9	31:0	6Ch	5th Fail address	User defined Late data [71:64] & Early data [71:64]	Word4 Circular shift data	LFSR random Late data [71:64] & Early data [71:64]	User defined Late data [71:64] (2nd burst data) & Early data [71:64] (2nd burst data)
MBDATA8	31:0	68h	Late data [71:64] & Early data [71:64] Failure bit location accumulator	5th Fail address Or Late data [71:64] & Early data [71:64] Failure bit location accumulator	5th Fail address Or Late data [71:64] & Early data [71:64] Failure bit location accumulator	5th Fail address Or Late data [71:64] & Early data [71:64] Failure bit location accumulator	User defined Late data [71:64] (1st burst data) & Early data [71:64] (1st burst data)
MBDATA7	31:0	64h	Fail address 4	User defined Late data [63:32]	DW3 Circular shift data	LFSR random Late data [63:32]	User defined Late data [63:32] (2nd burst data)
MBDATA6	31:0	60h	Fail address 3	User defined Late data [31:0]	DW2 Circular shift data	LFSR random Late data [31:0]	User defined Late data [31:0] (2nd burst data)
MBDATA5	31:0	5Ch	Fail address 2	User defined Early data [63:32]	DW1 Circular shift data	LFSR random Early data [63:32]	User defined Early data [63:32] (2nd burst data)
MBDATA4	31:0	58h	Fail address 1	User defined Early data [31:0]	DW0 Circular shift data	LFSR random Early data [31:0]	User defined Early data [31:0] (2nd burst data)
MBDATA3	31:0	54h	Late data [63:32] Failure bit location accumulator	Fail address 4 Or Late data [63:32] Failure bit location accumulator	Fail address 4 Or Late data [63:32] Failure bit location accumulator	Fail address 4 Or Late data [63:32] Failure bit location accumulator	User defined Late data [63:32] (1st burst data)
MBDATA2	31:0	50h	Late data [31:0] Failure bit location accumulator	Fail address 3 Or Late data [31:0] Failure bit location accumulator	Fail address 3 Or Late data [31:0] Failure bit location accumulator	Fail address 3 Or Late data [31:0] Failure bit location accumulator	User defined Late data [31:0] (1st burst data)
MBDATA1	31:0	4Ch	Early data [63:32] Failure bit location accumulator	Fail address 2 Or Early data [63:32] Failure bit location accumulator	Fail address 2 Or Early data [63:32] Failure bit location accumulator	Fail address 2 Or Early data [63:32] Failure bit location accumulator	User defined Early data [63:32] (1st burst data)
MBDATA0	31:0	48h	Early data [31:0] Failure bit location accumulator	Fail address 1 Or Early data [31:0] Failure bit location accumulator	Fail address 1 Or Early data [31:0] Failure bit location accumulator	Fail address 1 Or Early data [31:0] Failure bit location accumulator	User defined Early data [31:0] (1st burst data)

\* In the later half part of data burst length 8 test, 144 bits or 288 bits user-defined data pattern will be repeat as the same sequence of burst length 4.

### 11.5.1.3.1 MBDATA Failure Address Mapping

To compress the failure address into 32 bits, bits that are always zero are removed from the logging. These removed bits include AutoPrecharge Column address [10] and least significant bits assumed by burst length.

**Table 42 — MBDATA Failure Address Register Correspondence to DRAM Address**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	see description below												
Bank			Row																Column and Chunk												

BL4: 1 bit chunk indicates the location of 2 failure burst data chunks.

The above Column plus Chunk is equal to DRAM column address as the following:

**Table 43 — BL4 Column and Chunk Correspondence to DRAM Address**

Register Bit Location	12	11	10	9	8	7	6	5	4	3	2	1	0	
DRAM Col Address	14	13	12	11	9	8	7	6	5	4	3	2		
Data Chunk													1	X

- where the auto-precharge address bit 10 is assumed zero
- since data is logged in 144 bits (two chunks), address bit zero is not needed

BL8: 2 bit chunk indicates the location of 4 failure burst data chunks.

The above Column plus Chunk is equal to DRAM column address as the following:

**Table 44 — BL8 Column and Chunk Correspondence to DRAM Address**

Register Bit Location	12	11	10	9	8	7	6	5	4	3	2	1	0	
DRAM Col Address	14	13	12	11	9	8	7	6	5	4	3			
Data Chunk												2	1	X

- where the auto-precharge address bit 10 is assumed zero
- since data is logged in 144 bits (two chunks), Data chunk address bit zero is not needed

### 11.5.1.4 MB\_START\_ADDR: Memory Test Start Address

MB\_END\_ADDR row and column address must be larger than MB\_START\_ADDR row and column address in either increasing or decreasing address mode.

During FastX, FastY and FastXY operation, only one memory bank will be selected. User should only define the desired bank in MB\_START\_ADDR[2:0]. MB\_END\_ADDR[2:0] is ignored.

This register is only used when MBCSR.atype = 2b'10, and when MBCSR.algo is non-zero.

**11.5.1.4 MB\_START\_ADDR: Memory Test Start Address (cont'd)**

Function:3 Offset:9Ch			
Bit	Attr	Default	Description
31:16	RWST	0000h	ROW: MemBIST Start Row Address 15:0
15	RV	0	Reserved
14:3	RWST	0000h	COL: MemBIST Start Column Address BL8 [14:3] <==> Column Address 15:11, 9:3 BL4 [14:3] <==> Column Address 14:11, 9:2
2:0	RWST	000	BA: MemBIST Start Bank Address 2:0

**11.5.1.5 MB\_END\_ADDR: Memory Test End Address**

This register is only used when MBCSR.atype = 2b'10, and when MBCSR.algo is non-zero.

Function:3 Offset:A0h			
Bit	Attr	Default	Description
31:16	RWST	0000h	ROW: MemBIST End Row Address 15:0
15	RV	0	Reserved
14:3	RWST	0000h	COL: MemBIST End Column Address BL8 [14:3] <==> Column Address 15:11, 9:3 BL4 [14:3] <==> Column Address 14:11, 9:2
2:0	RWST	000	BA: MemBIST End Bank Address 2:0

**11.5.1.6 MBLFSRSED: Memory Test Circular Shift and LFSR Seed**

Function:3 Offset:A4h			
Bit	Attr	Default	Description
31:0	RWST	0000h	DMBLFSRSED:MemBIST LFSR Seed This 32 bit register will be used as the initial data seed for LFSR or Circular shift data pattern.

**11.5.1.7 MBFADDRPTR: Memory Test Failure Address Pointer Register**

Function:3 Offset:A8h			
Bit	Attr	Default	Description
31:0	RWST	0000h	<p>DMBFADDRPTR: This 32 bit register designates which MemBIST failures to log in the available failure address locations.</p> <p>The default value of this register is zero. It means MemBIST always starts logging on the first failure address. If it is programmed to hex A (10 in decimal), MemBIST will log failure addresses starting from the 11th failure. The corresponding MB_ERR_DATA0 register will log corrupted data in the first designated failure address.</p> <p>Note: this register does not affect the MBDATA failure bit location accumulators.</p>

**11.5.1.8 MB\_ERR\_DATA00: Memory Test Error Data 0 Bytes [3:0]**

Stores the first 32 bits of the 1st 144 bit failure data

Function:3 Offset:B0h			
Bit	Attr	Default	Description
31:0	RWST	0000h	<p>DATA: Early failure data [31:0]</p> <p><b>Note:</b> Read/Write for firmware debug purposes ONLY</p>

**11.5.1.9 MB\_ERR\_DATA01: Memory Test Error Data 0 Bytes [7:4]**

Stores the second 32 bits of the 1st 144 bit failure data

Function:3 Offset:B4h			
Bit	Attr	Default	Description
31:0	RWST	0000h	<p>DATA: Early failure data [63:32]</p> <p><b>Note:</b> Read/Write for firmware debug purposes ONLY</p>



**11.5.1.10 MB\_ERR\_DATA02: Memory Test Error Data 0 Bytes [11:8]**

Stores the third 32 bits of the 1st 144 bit failure data

Function:3 Offset:B8h			
Bit	Attr	Default	Description
31:0	RWST	0000h	DATA: Late failure data [31:0] <b>Note:</b> Read/Write for firmware debug purposes ONLY

**11.5.1.11 MB\_ERR\_DATA03: Memory Test Error Data 0 Bytes [15:12]**

Stores the fourth 32 bits of the 1st 144 bit failure data

Function:3 Offset:BCh			
Bit	Attr	Default	Description
31:0	RWST	0000h	DATA: Late failure data [63:32] <b>Note:</b> Read/Write for firmware debug purposes ONLY

**11.5.1.12 MB\_ERR\_DATA04: Memory Test Error Data 0 Bytes [17:16]**

Stores the last 16 bits of the 1st 144 bit failure data

Function:3 Offset:C0h			
Bit	Attr	Default	Description
15:0	RWST	0000h	DATA: Late failure data [71:64] & Early failure data [71:64] <b>Note:</b> Read/Write for firmware debug purposes ONLY

## 11.5.2 Memory Registers

### 11.5.2.1 DAREFTC: DRAM Auto-Refresh Timing and Control

Function:3 Offset:70h			
Bit	Attr	Default	Description
31:24	RV	0	Reserved
23:16	RWST	4Eh	TRFC: DRAM refresh period
15	RW	0	AREFEN: auto-refresh enable <b>Note:</b> This bit can also be cleared by the AMB self-refresh FSM as described in section 3.5.1
14:0	RWST	0C30h	TREFI: DRAM refresh interval

### 11.5.2.2 DSREFTC: DRAM Self-Refresh Timing and Control

Function:3 Offset:74h			
Bit	Attr	Default	Description
23:17	RV	0	Reserved
16	RWST	1	<b>DISSREXIT:</b> Disable DRAM Self-Refresh Exit when the link comes up
15:8	RWST	56h	<b>TXSNR:</b> DRAM Self-Refresh Exit to Non-Read Command Timing
7:4	RWST	Fh	TRP: DRAM Precharge Timing
3	RV	0	Reserved
2:0	RWST	7h	<b>TCKE:</b> DRAM Minimum CKE Pulse Width

### 11.5.2.3 MTR: Memory Technology Register

This register provides a local definition of the organization of DIMMs.

**Note:** These registers shall be copied from the SPD.

Function:3 Offset:77h			
Bit	Attr	Default	Description
7	RV	0	<i>Reserved</i>
6	RWST	0	WIDTH: Technology – DRAM data width Define the data width of SDRAMs within these DIMM's 0 = x4 (4 bits wide) 1 = x8 (8 bits wide)
5	RWST	0	NUMRANK: Technology – Number of Ranks Define the number of ranks within these DIMM's 0 = single ranked 1 = double ranked
4	RWST	0	NUMBANK: Technology – Number of Banks Define the number of banks within these DIMM's 0 = 4 banks 1 = 8 banks
3:2	RWST	00	NUMROW: Technology – Number of Rows Define the number of rows within these DIMM's 00 = 8,192 01 = 16,384 10 = 32,768 11 = 65,536
1:0	RWST	00	NUMCOL: Technology – Number of Columns Define the number of columns within these DIMM's 00 = 1,024 01 = 2,048 10 = 4,096 11 = 8,192

**11.5.2.4 DRT: DRAM Timing Control****DRAM Timing Control Table**

Function:3 Offset:78h			
Bit	Attr	Default	Description
31	RV	0	<i>Reserved</i>
30:29	RWST	00	<p>TRAS: DRAM tRAS minimum required delay from active command to precharge command. Delay cycles based on JEDEC DDRII spec 45 ns for DDRII 400/533/667. Based on the latest JEDEC spec (JESD79-2, Sept 2003) for DDRII 800 MHz min tRAS is not defined yet.</p> <p>tRASMIN clocks delay:</p> <p>00 =&gt; 18 for DDRII 800 MHz</p> <p>01 =&gt; 15 for DDRII 667 MHz</p> <p>10 =&gt; 12 for DDRII 533 MHz</p> <p>11 =&gt; Reserved</p>
28:27	RWST	00	<p>TRTP: DRAM cell internal read to precharge command delay.</p> <p>tRTP clocks delay:</p> <p>00 =&gt; 2</p> <p>01 =&gt; 3</p> <p>10 =&gt; 4</p> <p>11 =&gt; 5</p>
26:24	RWST	000	<p>BBRW: Back to Back Read-Write turn around.</p> <p>This field determines the minimum number of CMDCLK between Read-Write commands. The purpose of these 3 bits are to control the turnaround time on the DQ bus.</p> <p>Regular setting will be based on <math>BL/2 + 2 \text{ tCK}</math>.</p> <p>BL4: tR2W = 4 tCK</p> <p>BL8: tR2W = 6 tCK</p> <p>Command clocks apart based on the following encoding:</p> <p>000 =&gt; 10</p> <p>001 =&gt; 9</p> <p>010 =&gt; 8</p> <p>011 =&gt; 7</p> <p>100 =&gt; 6</p> <p>101 =&gt; 5</p> <p>110 =&gt; 4</p> <p>111 =&gt; 3 (stress mode, not recommended)</p>
23	RV	0	<i>Reserved</i>

**DRAM Timing Control Table (Continued)**

Function:3 Offset:78h			
Bit	Attr	Default	Description
22:20	RWST	000	<p>BBWR: Back to Back Write-Read turn around.</p> <p>This field determines the minimum number of CMDCLK between Write-Read commands. The purpose of these 3 bits are to control the turnaround time on the DQ bus.</p> <p>Regular setting will be based on <math>(CL-1)+BL/2+tWTR</math>.</p> <p>Command clocks apart based on the following encoding:</p> <p>000 =&gt; 12  001 =&gt; 11  010 =&gt; 10  011 =&gt; 9  100 =&gt; 8  101 =&gt; 7  110 =&gt; 6  111 =&gt; 5 (stress mode, not recommended)</p>
19	RV	0	Reserved
18:16	RWST	000	<p>TWR: Twr DRAM Write Recovery delay</p> <p>Overall delay clocks will be <math>(CL+AL-1) + BL/2 + tWR</math> from write command to precharge command.</p> <p>000 =&gt; 9  001 =&gt; 8  010 =&gt; 7  011 =&gt; 6  100 =&gt; 5  101 =&gt; 4  110 =&gt; 3  111 =&gt; 2</p>

**DRAM Timing Control Table (Continued)**

<b>Function:3 Offset:78h</b>			
<b>Bit</b>	<b>Attr</b>	<b>Default</b>	<b>Description</b>
15:12	RWST	0000	TRC: Trc DRAM activate to another activate delay 0000 => 26 0001 => 25 0010 => 24 0011 => 23 0100 => 22 0101 => 21 0110 => 20 0111 => 19 1000 => 18 1001 => 17 1010 => 16 1011 => 15 1100 => 14 1101 => 13 1110 => 12 1111 => 11
11:10	RWST	00	TRCD: Trcd DRAM RAS# to CAS# delay 00 => 6 01 => 5 10 => 4 11 => 3  If AL >= Trcd, Read/Write command will be issued right after ACT cycle.
9:8	RWST	00	TRP: Trp DRAM RAS# to Precharge delay 00 => 6 01 => 5 10 => 4 11 => 3
7:0	RWST	00h	NOPCNT: Programmable NOP insertion (Device Deselect actually). Number of Nops will be inserted between read/write commands to slow down MemBIST activities. Up to 255 clocks NOPs can be programmed to insert delay between read/write commands. If NOPs delay is programmable less than the required DRAM timing, Overall NOP delay from command to command will not be seen.

### 11.5.2.5 DRC: DRAM Controller Mode Register

This register controls the mode of the DRAM Controller.

**DRAM Controller Mode Register Table**

Function:3 Offset:7Ch			
Bit	Attr	Default	Description
31:30	RV	00	Reserved
29	RW	0	<b>INITDONE: Initialization Complete.</b> This scratch bit communicates software state from the AMB to BIOS. BIOS sets this bit to 1 after initialization of the DRAM memory array is complete. This bit has no effect on AMB operation.
28	RV	0	Reserved
27:24	RWST	0	<b>CLKDIS:</b> clock[3:0] output disable
23	RWST	0	<b>SEQADDR:</b> When set to 1 turns off address balancing to support DRAMs programmed for Sequential Burst Type
19:22	RV	00	Reserved
18	RWST	1	<b>ODTZ: On-Die Termination Strength.</b> “0” Disabled “1” Enabled
17	RWST	0	<b>HLDDIS:</b> command/address hold disable
16	RWST	0	<b>BALDIS:</b> command/address balancing disable
15	RW	0	<b>CADIS:</b> command/address output disable
14	RW	0	<b>CSDIS:</b> chip select output disable
13	RW	0	<b>ODTDIS:</b> ODT output disable
12	RWST	1	<b>CKEFRCLW:</b> CKE Force Low Forces CKE low. Must be cleared to enable normal DDR functionality. This bit overrides the CKE1 and CKE0 fields described below, and also overrides all channel commands and other hardware functions that would otherwise affect the state of the CKE outputs.
11	RW	0	<b>CKEDIS:</b> CKE output disable
10	RWST	0	<b>CKE1:</b> CKE output 1 control and status. Software can write to this bit to change the state of the CKE 1 output. Hardware will update this bit with the current status of the CKE1 output two core cycles after a channel command or other hardware function changes the state of the CKE1 output. ‘1’ = CKE1 pads asserted. ‘0’ = CKE1 pads de-asserted.
9	RWST	0	<b>CKE0:</b> CKE output 0 control and status. Software can write to this bit to change the state of the CKE 0 output. Hardware will update this bit with the current status of the CKE 0 output two core cycles after a channel command or other hardware function changes the state of the CKE 0 output. ‘1’ = CKE0 pads asserted. ‘0’ = CKE0 pads de-asserted.

**DRAM Controller Mode Register Table (Continued)**

<b>Function:3 Offset:7Ch</b>			
<b>Bit</b>	<b>Attr</b>	<b>Default</b>	<b>Description</b>
8	RWST	0	<b>BL</b> : DRAM burst length. ‘1’ = bl8 ‘0’ = bl4
7:4	RWST	2h	<b>AL</b> : DRAM Additive Latency [3:0]
3:0	RWST	3h	<b>CL</b> : DRAM CAS Latency [3:0]

**11.5.3 Thermal Sensor Registers****11.5.3.1 TEMPLO: Temperature Low Trip Point**

Low trip point.

<b>Function:3 Offset:80h</b>			
<b>Bit</b>	<b>Attr</b>	<b>Default</b>	<b>Description</b>
7:0	RWST	FFh	TEMPLO: Low threshold trip point

**11.5.3.2 TEMPMID: Temperature Mid Trip Point**

Mid trip point.

<b>Function:3 Offset:81h</b>			
<b>Bit</b>	<b>Attr</b>	<b>Default</b>	<b>Description</b>
7:0	RWST	FFh	TEMPMID: Mid threshold trip point

**11.5.3.3 TEMPHI: Temperature High Trip Point**

High trip point.

<b>Function:3 Offset:82h</b>			
<b>Bit</b>	<b>Attr</b>	<b>Default</b>	<b>Description</b>
7:0	RWST	FFh	TEMPHI: High threshold trip point



**11.5.3.4 UPDATED: Update Temp Diff Bit**

Take new temperature sample and update the temp diff bit (INCREASING).

<b>Function:3</b> <b>Offset:83h</b>			
<b>Bit</b>	<b>Attr</b>	<b>Default</b>	<b>Description</b>
7:1	RV	00h	reserved
0	RWS	0	UPDATE: Write '1' = latch current temperature (TEMP) and update INCREASING bit of TEMPSTAT register; Automatically clears this bit to '0' after INCREASING bit is updated; Write '0' - no effect

### 11.5.3.5 TEMPSTAT: Thermal Sensor Status Register

This register controls and reports temperature status.

Function:3 Offset:84h			
Bit	Attr	Default	Description
7:6	RV	0	Reserved
5	RWST	0	NoAutoUpdate '1' = turns off update of temp stat values so that forced values written in by firmware are not overwritten '0' = trip registers automatically updated as normal
4	RW	0	<b>INCREASING</b> '1' = Temperature has increased since the last time UPDATE bit was set in UPDATED register. '0' = Temperature has not increased since the last time UPDATE bit was set in UPDATED register. This is reflected as the Rising/Falling value in the Thermal Trip field of northbound FBD status 0.
3	RWST	0	<b>OVERTEMPHI</b> '1' = Temperature is above or equal to TEMPHI.TRIP '0' = Temperature is below TEMPHI.TRIP
2	RWST	0	<b>OVERTEMPMID</b> '1' = Temperature is above or equal to TEMPMID.TRIP '0' = Temperature is below TEMPMID.TRIP This is reflected in the Thermal Trip value of northbound FBD status 0
1	RWST	0	<b>OVERTEMPLO</b> '1' = Temperature is above or equal to TEMPLO.TRIP '0' = Temperature is below TEMPLO.TRIP This is reflected in the Thermal Trip value of northbound FBD status 0
0	RWST	0	<b>TEMPHIENABLE</b> '1' = Allow OVERTEMPHI=1 to shut down the DDR channel, drop DDR commands, log an error, and take FBD links to EI. '0' = OVERTEMPHI=1 only logs an error.

#### Notes:

1. The OVERTEMPLO, OVERTEMPMID and OVERTEMPHIGH bits of the TEMPSTAT register are refreshed whenever TEMP has a new value. This is independent of the UPDATE bit in the UPDATED register.
2. TEMPSTAT[3:1] = 000, when temperature is below TEMPLO.TRIP.
3. TEMPSTAT[3:1] = 001, when temperature is above or equal to TEMPLO.TRIP but below TEMPMID.TRIP.
4. TEMPSTAT[3:1] = 011, when temperature is above or equal to TEMPMID.TRIP but below TEMPHIGH.TRIP.
5. TEMPSTAT[3:1] = 111, when temperature is above or equal to TEMPHIGH.TRIP

### 11.5.3.6 TEMP: Temperature A/D

Current temperature reading. This- 8-bit with 0.5 degree resolution is continuously and automatically kept up to date by AMB hardware.

Function:3 Offset:85h			
Bit	Attr	Default	Description
7:0	RO	00h	DEGREES: Current temperature - binary encode 0 - 127 °C

## 11.6 Implementation Specific DDR Initialization and Calibration Registers (Function 4)

### 11.6.1 DDR Calibration

#### 11.6.1.1 DCALCSR: DCAL Control and Status

Function:4 Offset:40h			
Bit	Attr	Default	Description
31	RWS	0	<b>START: Start Operation</b> When set to 1 by software, the operation selected by the dcalcsr.opcode is initiated. Hardware clears this bit when the operation is complete.
30:28	RW	0	<b>FAIL: Completion Status</b> 1xx = Fail, 0xx = Pass <b>Note:</b> Read/Write for firmware debug purposes ONLY
27:23	RV	00	Reserved
22:21	RW	00	CS: Rank select This field corresponds to the chip select outputs: CS[1:0]. Setting a bit in this field will cause the corresponding CS pin to drive low when commands are issued on the DDR bus. This field Applies to NOP, Refresh, Precharge all, and MRS/EMRS commands.
20:15	RV	00	Reserved
14:4	RW	000h	<b>OPMODS:</b> Operation modifiers
3:0	RW	0h	<b>OPCODE:</b> “0000” = NOP “0001” = Refresh “0010” = Pre-Charge “0011” = MRS/EMRS “0101” = Automatic DQS Delay Calibration “1100” = Automatic Receive Enable Calibration “1101” = Self-Refresh Entry All other settings are reserved

11.6.1.2 DCALADDR: DCAL Address Register

<b>Function:4</b> <b>Offset:44h</b>			
Bit	Attr	Default	Description
31:0	RW	0000_0000h	<b>DCALADDR: DCAL Address and Other Information Based on Opcode.</b>

Table 45 — Functional Characteristics of DCALADDR

Bit	NOP, Refresh, Pre-Charge, MRS/ EMRS, and Self-Refresh Entry Commands initiated by DCALCSR
31	DRAM Address Bus 15:0
30	
29	
28	
27	
26	
25	
24	
23	
22	
21	
20	
19	
18	
17	
16	
15	
14	
13	
12	
11	
10	
9	
8	
7	
6	
5	
4	
3	
2	DRAM Bank Address Bus 2:0
1	
0	

### 11.6.1.3 S3RESTORE [15:0] : DDR State Restore

These registers contain implementation dependent state needed to recover connections to DRAMs left in self refresh without destroying data in the DRAMs. For example, these may contain calibration information for DDR IO drivers. BIOS will copy these registers into some form of stable storage prior to system standby then restore these registers after system wakes up.

**Note:** The functionality of the AMB S3 restore registers is design dependent. Some of the S3 restore registers may or may not be implemented depending the AMB design.

Function:4 Offset:E0h - A4h			
Bit	Attr	Default	Description
31:0	RWST	00	S3STATE:

### 11.6.1.4 DDR2ODTC: DDR2 DRAM On-Die Termination Control

The DDR2ODTC controls the behavior of the ODT output (one ODT output per command bus copy). There is a separate field to control the behavior for reads to rank0, reads to rank1, writes to rank0, and writes to rank1. Only the lsb of each field is used, and the msb has no effect. When an lsb of a field is set to one, the ODT pins will drive high, at the appropriate time relative to data on the DDR bus, when the selected transaction (read or write) is issued to the selected rank (0 or 1.). If a field is set to 0, the ODT output continues to drive low during the transaction, as it does during idle cycles.

Function:4 Offset:FCh			
Bit	Attr	Default	Description
7:6	RWST	0h	R1ODTWR: ODT control during writes to CS1 x1: ODT pins will drive high x0: ODT pins remain driving low
5:4	RWST	0h	R1ODTRD: ODT control during reads to CS1
3:2	RWST	0h	R0ODTWR: ODT control during writes to CS0
1:0	RWST	0h	R0ODTRD: ODT control during reads to CS0

## 11.7 DFX Registers (Function 5)

### 11.7.1 Transparent Mode Registers

#### 11.7.1.1 TRANSCFG: Transparent Mode Configuration

This register enables and controls FBD DFX transparent mode features.

Function:5 Offset:3Ch			
Bit	Attr	Default	Description
31:29	RV	0h	Reserved
28	RWST	0	ENDOUT: enable data output on transparent data/status pins when set, output status when clear
27	RWST	0	LGFBITS: log bits that fail the compare when set, log raw read data when clear.
26	RWST	0	LGFFAIL: log first failure in any burst position.
25:24	RWST	00	BSTPOS: burst position to log data/failed bits from when LGFFAIL bit is not set. 0 = first burst in bl4 or bl8 mode 1 = last burst of bl4, second burst of bl8 2 = third burst of bl8 3 = last burst of bl8
23:20	RWST	0h	DRAMRD: byte of data bus selected to be output on transparent data/status pins when ENDOUT bit is set. 8= DQS 17 and DQS 8 7= DQS 16 and DQS 7 ... 0 = DQS 9 and DQS 0
19:16	RWST	0h	DRAMWR: byte of data bus selected to receive transparent write data, and byte of data bus to be compared against transparent read data. Fh = all bytes 8= DQS 17 and DQS 8 7= DQS 16 and DQS 7 ... 0 = DQS 9 and DQS 0
15:0	RWST	0000h	DFTDATA: default data for bytes not selected by the DRAMWR field. This field has early/even data in the upper 8 bits, and late/odd data in the lower 8 bits.

### 11.7.1.2 TRANDERR[8:0]: Transparent Mode Data Error Logs

This register stores data returned from DRAM byte groups on failing transparent mode tests.

<b>Function:5</b> <b>Offset:50h, 4Eh, 4Ch, 4Ah, 48h,46h, 44h, 42h, 40h</b>			
Bit	Attr	Default	Description
15:8	RWST	00h	LATE_DATA: <b>Note:</b> Read/Write for firmware debug purposes ONLY
7:0	RWST	00h	EARLY_DATA: <b>Note:</b> Read/Write for firmware debug purposes ONLY

### 11.7.1.3 TRANSCTRL: Transparent Mode Control

This register enables and controls FBD DFX transparent mode features.

<b>Function:5</b> <b>Offset:80h</b>			
Bit	Attr	Default	Description
7:1	RV	00h	Reserved
0	RWST	0	ENTRNSPMODE: Transparency Mode Enable 1 - Enables Transparency Mod

## 11.7.2 Logic Analyzer Interface (LAI) Registers

This block of registers describe the optional LAI mode for AMBs.

### 11.7.2.1 LAI: LAI Operation Modes

This register controls and reports the AMBs LAI mode and Qual controls.

Function:5 Offset:B8h			
Bit	Attr	Default	Description
31:16	RV	0000h	Reserved
15	RWST	0	<b>RAWMODE: data connected to LAI</b> 0: LAI outputs contain initialization state information <b>prior to L0S then lane data after L0S</b> 1: LAI outputs connected to FBD data inputs even though valid timing is not present
14	RV	0	Reserved
13	RWST	0	<b>QUALMODE:</b> Assert Qual for all non-filtered frames, or only assert Qual for all non-filtered frames between start and stop events. 0: Ignore Qual start/stop events 1: Assert Qual after a start event, and deassert Qual after a stop events
12	RWST	0	<b>FILTERSYNC:</b> Filter the frame (do not assert Qual) if the frame is a sync. 0: Disable sync filtering 1: Enable sync filtering
11:6	RV	00h	Reserved
5:0	RWST	3Fh	<b>QUALPERIOD:</b> Additional number of frames Qual remains asserted Power-on default to 63

### 11.7.2.2 SBMATCHU: Upper Southbound Match Register

This register sets the upper 8 bits of data match for three southbound commands.

Function:5 Offset:BCh			
Bit	Attr	Default	Description
31:2 4	RV	00h	Reserved
23:1 6	RWST	00h	<b>CMD2:</b> Upper 8 bits [39:32] of southbound command 2
15:8	RWST	00h	<b>CMD1:</b> Upper 8 bits [39:32] of southbound command 1
7:0	RWST	00h	<b>CMD0:</b> Upper 8 bits [39:32] of southbound command 0



### 11.7.2.2 SBMATCHU: Upper Southbound Match Register (cont'd)

Match and Mask bit numbering of SB frames is as follows:

- where N= 0 for slot A, 4 for slot B and 8 for slot C

**Table 46 — Bit Locations for SB Match and Mask**

Xfr\lane	9	8	7	6	5	4	3	2	1	0
0 + N	B36	B32	B28	B24	B20	B16	B12	B8	B4	B0
1 + N	B37	B33	B29	B25	B21	B17	B13	B9	B5	B1
2 + N	B38	B34	B30	B26	B22	B18	B14	B10	B6	B2
3 + N	B39	B35	B31	B27	B23	B19	B15	B11	B7	B3

### 11.7.2.3 SBMATCHL0: Lower Southbound Match Register 0

This register sets the lower 32 bits of data match for match southbound command 0.

Function:5 Offset:C0h			
Bit	Attr	Default	Description
31:0	RWST	00004000h	<b>CMD:</b> Lower 32bits [31:0] of southbound command power on default = match Synch

### 11.7.2.4 SBMATCHL1: Lower Southbound Match Register 1

This register sets the lower 32 bits of data match for match southbound command 1.

Function:5 Offset:C4h			
Bit	Attr	Default	Description
31:0	RWST	00100000h	<b>CMD:</b> Lower 32bits [31:0] of southbound command power on default = match Activate

### 11.7.2.5 SBMATCHL2: Lower Southbound Match Register 2

This register sets the lower 32 bits of data match for match southbound command 2.

Function:5 Offset:C8h			
Bit	Attr	Default	Description
31:0	RWST	00014000h	<b>CMD:</b> Lower 32bits [31:0] of southbound command power on default = match Write Config Reg

**11.7.2.6 SBMASKU: Upper Southbound Mask Register**

This register sets the upper 8 bits of data mask for three southbound commands.

<b>Function:5</b> <b>Offset:CCh</b>			
<b>Bit</b>	<b>Attr</b>	<b>Default</b>	<b>Description</b>
31:24	RV	00h	Reserved
23:16	RWST	00h	<b>CMDMASK2:</b> Upper 8 bits [39:32] of southbound command 2 mask 0: Do not include this bit in match comparison 1: Include this bit in match comparison
15:8	RWST	00h	<b>CMDMASK1:</b> Upper 8 bits [39:32] of southbound command 1 mask 0: Do not include this bit in match comparison 1: Include this bit in match comparison
7:0	RWST	00h	<b>CMDMASK0:</b> Upper 8 bits [39:32] of southbound command 0 mask 0: Do not include this bit in match comparison 1: Include this bit in match comparison

**11.7.2.7 SBMASKL0: Lower Southbound Mask Register 0**

This register sets the lower 32 bits of data mask for match southbound command 0.

<b>Function:5</b> <b>Offset:D0h</b>			
<b>Bit</b>	<b>Attr</b>	<b>Default</b>	<b>Description</b>
31:0	RWST	031FC000h	<b>CMDMASK:</b> Lower 32bits [31:0] of southbound command mask. 0: Do not include this bit in match comparison 1: Include this bit in match comparison power on default = match Sync

**11.7.2.8 SBMASKL1: Lower Southbound Mask Register 1**

This register sets the lower 32 bits of data mask for match southbound command 1.

Function:5 Offset:D4h			
Bit	Attr	Default	Description
31:0	RWST	00100000h	<b>CMDMASK:</b> Lower 32bits [31:0] of southbound command mask. 0: Do not include this bit in match comparison 1: Include this bit in match comparison power on default = match Activate

**11.7.2.9 SBMASKL2: Lower Southbound Mask Register 2**

This register sets the lower 32 bits of data mask for match southbound command 2.

Function:5 Offset:D8h			
Bit	Attr	Default	Description
31:0	RWST	001FC000h	<b>CMDMASK:</b> Lower 32bits [31:0] of southbound command mask. 0: Do not include this bit in match comparison 1: Include this bit in match comparison power on default = match Write Config Reg

**11.7.2.10 MMEVENTSEL: Match/Mask Event Selection Register**

Selects 1 of 13 local match events described below for promotion to local event select. Three local events MMEVENT[2:0] can be associated with one of these local match events.

Function:5 Offset:DCh			
Bit	Attr	Default	Description
15:12	RV	0h	Reserved
11:8	RWST	2h	<b>MMEVENT2SEL:</b> default: match pattern 0 to slot A only for sync
7:4	RWST	Ah	<b>MMEVENT1SEL:</b> default: match pattern 1 to slot A , B or C for activate
3:0	RWST	3h	<b>MMEVENT0SEL:</b> default: match pattern 2 to slot B only for write config reg

**11.7.2.10 MMEVENTSEL: Match/Mask Event Selection Register (cont'd)****Table 47 — Local Mask and Match Events Selected by MMEVENTnSEL Fields**

<b>MM Event</b>	<b>Description</b>
15:13	Reserved
12	<b>FRAMEMATCH</b> Bit pattern in slot A matches SBMATCH/SBMASK 0 <b>AND</b> Bit pattern in slot B matches SBMATCH/SBMASK 1 <b>AND</b> Bit pattern in slot C matches SBMATCH/SBMASK 2
11	<b>SLOTMATCH0</b> Command in slot A, B, or C matches SBMATCH/ SBMASK 0
10	<b>SLOTMATCH1</b> Command in slot A, B, or C matches SBMATCH/ SBMASK 1
9	<b>SLOTMATCH2</b> Command in slot A, B, or C matches SBMATCH/ SBMASK 2
8	<b>SLOTCMATCH0</b> Command in slot C matches SBMATCH/SBMASK 0
7	<b>SLOTCMATCH1</b> Command in slot C matches SBMATCH/SBMASK 1
6	<b>SLOTCMATCH2</b> Command in slot C matches SBMATCH/SBMASK 2
5	<b>SLOTBMATCH0</b> Command in slot B matches SBMATCH/SBMASK 0
4	<b>SLOTBMATCH1</b> Command in slot B matches SBMATCH/SBMASK 1
3	<b>SLOTBMATCH2</b> Command in slot B matches SBMATCH/SBMASK 2
2	<b>SLOTAMATCH0</b> Command in slot A matches SBMATCH/SBMASK 0
1	<b>SLOTAMATCH1</b> Command in slot A matches SBMATCH/SBMASK 1
0	<b>SLOTAMATCH2</b> Command in slot A matches SBMATCH/SBMASK 2

**11.7.2.11 EVENTSEL0: Event Selection Register**

In LAI mode, selects 1 of 32 local events (see EVENT register) for 2 uses (Qual Start and Qual Stop) and sets programmable delay for QualStop. In Normal mode, selects local event for 2 uses (error injection and NB in-band event signaling) and sets programmable delay for error injection..

Function:5 Offset:E0h			
Bit	Attr	Default	Description
31:2 1	RV	00h	Reserved
20:1 5	RWST	3Fh	QUALSTOPDELAY: in LAI Mode Additional number of clocks QualStop is delayed before use (0 to 63) Power-on default to 63 INJERRORDELAY: in Normal Mode Additional number of clocks INJERROR is delayed before use (0 to 63) Power-on default to 63
14:1 0	RW	00h	INBAND: in LAI Mode No effect. Northbound in-band debug events can not be asserted in LAI mode INBAND: in Normal Mode If selected event occurs, assert the northbound in-band event bit in next sync status 0 return and in FBDS0.S3
9:5	RWST	00h	QUALSTART: in LAI Mode If selected event occurs, enable assertion of Qual until next QUALSTOP
4:0	RWST	00h	QUALSTOP: in LAI Mode <ul style="list-style-type: none"> <li>If selected event occurs, disable assertion of Qual until next QUALSTART</li> </ul> INJERROR: in Normal Mode <ul style="list-style-type: none"> <li>If selected event occurs, inject error selected by EICNTL</li> </ul>

**11.7.2.12 EVENTSEL1: Event Selection Register**

·Selects 1 of 32 local events (see EVENT register) for each of six events transmitted to the LAI interface (events[5:0]).

<b>Function:5 Offset:E4h</b>			
<b>Bit</b>	<b>Attr</b>	<b>Default</b>	<b>Description</b>
31:30	RV	00	Reserved
29:25	RWST	0Ah	LAITRIGGER5: Local event selected and transmitted to LAI as TRIGGER5 Default on power on to MM[1] event= Activate on any command
24:20	RWST	0Bh	LAITRIGGER4: Local event selected and transmitted to LAI as TRIGGER4 Default on power on to MM[2] event= Sync command in slot A
19:15	RWST	13h	LAITRIGGER3: Local event selected and transmitted to LAI as TRIGGER3 Default on power on to select in-band debug event 3
14:10	RWST	12h	LAITRIGGER2: Local event selected and transmitted to LAI as TRIGGER2 Default on power on to select in-band debug event 2
9:5	RWST	11h	LAITRIGGER1: Local event selected and transmitted to LAI as TRIGGER1 Default on power on to select in-band debug event 1
4:0	RWST	10h	LAITRIGGER0: Local event selected and transmitted to LAI as TRIGGER0 Default on power on to select in-band debug event 0

**11.7.2.13 EVENTSEL2: Event Selection Register**

Selects 1 of 32 local events (see EVENT register) for each of five events transmitted to the LAI interface (events[10:6]).

<b>Function:5 Offset:E8h</b>			
<b>Bit</b>	<b>Attr</b>	<b>Default</b>	<b>Description</b>
31:30	RV	00	Reserved
29:25	RV	00h	Reserved
24:20	RWST	04h	LAITRIGGER10: Local event selected and transmitted to LAI as TRIGGER10 Default on power on to SB Unit Testing State detect
19:15	RWST	1Ah	LAITRIGGER9: Local event selected and transmitted to LAI as TRIGGER9 Default on power on to SB CRC error detect
14:10	RWST	0Dh	LAITRIGGER8: Local event selected and transmitted to LAI as TRIGGER8 Default on power on to Event Bus[1] event
9:5	RWST	0Ch	LAITRIGGER7: Local event selected and transmitted to LAI as TRIGGER7 Default on power on to Event Bus[0] event
4:0	RWST	09h	LAITRIGGER6: Local event selected and transmitted to LAI as TRIGGER6 Default on power on to MM[0] event= Write Register in command slot B

**11.7.2.14 EVENT: Local LAI Event Register**

This register sets a bit if a local event is hit. Except for QUAL, event signal internal to the AMB will only toggle one cycle when bit is set to avoid multiple triggers per event. The 5-bit encoding for the bit number is used by the EVENTSEL register to select the event corresponding to the bit number.

<b>Function:5 Offset:F0h</b>			
<b>Bit</b>	<b>Attr</b>	<b>Default</b>	<b>Description</b>
31	RWCST	0	Spare:
30:25	RWCST	00h	ERROR EVENTS: <ul style="list-style-type: none"> <li>• SB/NB failover[25],</li> </ul> when unmasked: <ul style="list-style-type: none"> <li>• SB CRC error[26],</li> <li>• thermal overload[27],</li> <li>• clock training violation (&lt; 6 transitions in 512 UI) [28],</li> <li>• unimplemented register access[29],</li> <li>• other implementation specific errors[30]</li> </ul> set on event and cleared by writing
24	RWCST	0	QUALFLAG:
23:16	RWCST	00h	INBANDEV: SB link in-band EV[7:0] set on event and cleared by writing
15:12	RWCST	0h	EV: Event Bus EV[3:0] set on event and cleared by writing
11:9	RWCST	0h	MMEVENT: MMEVENT[2:0] selected by MMEVENTSEL set on event and cleared by writing
8:1	RWST	0h	LINKST: FBD Link State: Disable[1], calibrate[2], training[3], testing[4], polling[5], config[6], 10[7], 10s or recalibrate[8] One hot encoding of FBD link state
0	RO	0	NULL: Null Event: Bit never set



**11.7.2.15 EVBUS: Event Bus Control Register**

EBUS fields select 1 of 32 local events (see EVENT register) for output to the GBAMB event bus. EVTYPE sets up type of event for each event bus pin and EVT fields set event bus timing filters.

<b>Function:5</b> <b>Offset:F4h</b>			
<b>Bit</b>	<b>Attr</b>	<b>Default</b>	<b>Description</b>
31:27	RWST	00h	EBUS3: Local event selected for event bus [3]
26:22	RWST	00h	EBUS2: Local event selected for event bus [2]
21:17	RWST	03h	EBUS1: Local event selected for event bus [1] default on power-on = start of initialization as detected by Init Training State Event
16:12	RWST	17h	EBUS0: Local event selected for event bus [0] default on power-on = In-band Debug Event 7 (23d)
11:8	RWST	0h	EVTYPE: 0 = pulse event 1 = level event bit 11 for EVBUS3 thru bit 8 for EVBUS0
7:0	RWST	0Fh	EVT1: Min delay after EVBus trigger out deasserted before next assertion allowed and same value is used for Pulse width used when asserting all EVBus outputs Power on default of 16 clks

### 11.7.3 Error Injection Registers

#### 11.7.3.1 EICNTL: Error Injection Control

This register controls the AMBError injection logic.

Function:5 Offset:FCh			
Bit	Attr	Default	Description
7	RW	0	<b>EIEN:Error Injection Enable</b> 1= Error Injection enabled 0= Error Injection disabled
6:4	RW	000	<b>EITYPE: Type of error injection</b> 111 = Reserved; 110 = Reserved 101 = Force NB Error bit on next Status return 100 = Force Alert on event 011 = Reserved 010 =Reserved 001= Corrupt NB CRC on event 000= No error injection
3:0	RV	0h	Reserved

#### 11.7.3.2 STUCKL: Stuck “ON” FBD Lanes

This register selects FBD Lanes to be stuck at EI following next link reset.

Function:5 Offset:FEh			
Bit	Attr	Default	Description
7:4	RV	0h	Reserved
3:0	RWST	Fh	<b>NBSTUCK: NB Lane to be driven to EI to simulate a failed lane</b> <ul style="list-style-type: none"> <li>0h = lane 0: Dh = lane 13 and &gt; 13 = NOP</li> </ul>

### 11.8 Bring-up and Debug Registers (Function 6)

#### 11.8.1 Southbound FBD IBIST Registers

##### 11.8.1.1 SBFIBPORTCTL: Southbound FBD IBIST Port Control Register

This register controls the operation of the IBIST logic.

**11.8.1.1 SBFIBPORTCTL: Southbound FBD IBIST Port Control Register (cont'd)****Southbound FBD IBIST Port Control Register Table**

<b>Device:NodeID</b> <b>Function: 6</b> <b>Offset:80h</b>			
<b>Bit</b>	<b>Attr</b>	<b>Default</b>	<b>Description</b>
31:24	RV	00h	Reserved
23	RWST	0	SBNBMAP: Loopback mapping bit This bit will be sent during TS1 to the target to specify which lanes needs to be looped back. Actual lanes looped back is specified in the FBD Architecture Spec.
22	RWST	0	CMMSTR: Compliance Measurement Mode start This puts the IBIST logic in CMM mode and IBIST TX engine will start transmitting IBIST patterns.
21:12	RWCST	000h	ERRCNT: Error Counter Total number of errors encountered in this port.
11:8	ROST	0h	ERLNNUM: Error Lane Number This points to the first lane that encountered an error. If more than one lane reports an error in a cycle, the most significant lane number that reported the error will be logged.
7:6	RWCST	00	ERRSTAT: Port Error Status When IBIST is started, status goes to 01 until first start delimiter is received and then goes to 00 until the end or to 10 if an error occurs. 00: No error. 01: Did not receive first start delimiter. 10: Transmission error (first error). 11: Reserved for future use
5	RWST	0	AUTOINVSWPEN: Auto Inversion sweep enable This bit enables the inversion shift register to continuously rotate the pattern in the FIBTXSHFT and FIBRXSHFT registers. 0: Disable Auto-inversion 1: Enable Auto-inversions
4	RWST	0	STOPONERR: Stop IBIST on Error 0: Do not stop on error, only update error counter 1: Stop on error
3	RWST	0	LOOPCON: Loop forever 0: No looping 1: Loop forever
2	RWCST	0	COMPLETE: IBIST done flag 0: Not done 1: Done

**Southbound FBD IBIST Port Control Register Table (Continued)**

<b>Device:NodeID</b> <b>Function: 6</b> <b>Offset:80h</b>			
Bit	Attr	Default	Description
1	RWST	0	<b>MSTRMD: Controller Mode Enable</b> When this bit is set, during the next TS1 training set, IBIST will transmit patterns generated locally rather than looping back the incoming test data. 0: Disable Controller mode 1: Enable Controller mode
0	RWST	0	<b>IBISTR: IBIST Start</b> When set, IBIST starts transmitting after the TS1 header is recognized during the next link initialization sequence. and <b>MSTRMD</b> bit is set. This bit also enables the receive engine to start looking for the start delimiter during TS1 training set. This bit is reset when IBIST is done. The IBIST transmitter can be stopped by setting this bit to 0. 0: Stop IBIST transmitter 1: Start IBIST transmitter

**11.8.1.2 SBFIBPGCTL: SB IBIST Pattern Generator Control Register**

This register contains bits to control the operation of the IBIST pattern generator. All counts are in 24 bit increments.

**SB IBIST Pattern Generator Control Register Table**

<b>Device:NodeID</b> <b>Function: 6</b> <b>Offset:84h</b>			
Bit	Attr	Default	Description
31:26	RWST	0Fh	<b>OVRLLOOPCNT: Overall Loop Count</b> 0h: Reserved 1h:3Fh: Number of times to loop all the patterns.
25:21	RWST	00h	<b>CNSTGENCNT: Constant Generator Loop Counter</b> 00h: Disable constant generator output 01h: 1Fh The number of times the constant generator counter pattern should loop before going to the next component. Each count represents 24 bits of 1's or 0's.
20	RWST	0	<b>CNSTGENSET: Constant Generator Setting</b> 0: Generate 0 1: Generate 1
19:13	RWST	0Fh	<b>MODLOOPCNT: Modulo-N Loop Counter</b> Each count represents 24 bits of the pattern specified by <b>MODPERIOD</b> . 00h: Disable Pattern Output 01h: 7Fh The number of times the Pattern Buffer should loop before going to the next component.

**SB IBIST Pattern Generator Control Register Table (Continued)**

<b>Device:NodeID</b> <b>Function: 6</b> <b>Offset:84h</b>			
Bit	Attr	Default	Description
12:10	RWST	001b	MODPERIOD: Period of the Modulo-N counter Each encoding transmits a 24-bit pattern as specified below. All other encodings are reserved. 001: L/2 - 0101_0101_0101_0101_0101 010: L/4 - 0011_0011_0011_0011_0011 011: L/6 - 0001_1100_0111_0001_1100_0111 100: L/8 - 0000_1111_0000_1111_0000_1111 110: L/24 - 0000_0000_0000_1111_1111_1111
9:3	RWST	0Fh	PATTLOOPCNT: Pattern Buffer Loop Counter 00h: Disable Pattern Output 01h: 7Fh The number of times the Pattern Buffer ( <b>FIBPATTBUF1</b> ) should be repeated before going to the next component.
2:0	RWST	000	PTGENORD: Pattern Generation Order 000: Pattern Store + Modulo N Cntr + Constant Generator 001: Pattern Store + Constant Generator + Modulo N Cntr 010: Modulo N Cntr + Pattern Store + Constant Generator 011: Modulo N Cntr + Constant Generator + Pattern Store 100: Constant Generator + Pattern Store + Modulo N Cntr 101: Constant Generator + Modulo N Cntr + Pattern Store 110: Reserved 111: Reserved

**11.8.1.3 SBFIBPATTBUF1: SB IBIST Pattern Buffer 1 Register**

This register contains the pattern bits used in IBIST operations. Only the least significant 24 bits are used.

<b>Function: 6</b> <b>Offset:88h</b>			
Bit	Attr	Default	Description
31:24	RV	00h	Reserved
23:0	RWST	02ccfdh	IBPATBUF: IBIST Pattern Buffer Pattern buffer storing the default and the user programmable pattern. Default: 02ccfdh

**11.8.1.4 SBFIBTXMSK: SB IBIST Transmitter Mask Register**

This register enables IBIST operations for individual lanes. This mask only applies to transmitters and not receivers.

Function: 6 Offset:8Ch			
Bit	Attr	Default	Description
31:10	RV	000000h	Reserved
9:0	RWST	3FFh	TXMASK: Selects which channels to enable for testing.

**11.8.1.5 SBFIBRXMSK: SB IBIST Receiver Mask Register**

This register enables IBIST operations for individual lanes. This mask only applies to receivers and not transmitters.

Function: 6 Offset:90h			
Bit	Attr	Default	Description
31:10	RV	000000h	Reserved
9:0	RWST	3FFh	RXMASK: Selects which channels to enable for testing.

**11.8.1.6 SBFIBTXSHFT: SB IBIST Transmitter Inversion Shift Register**

Each bit in this register enables inverting the patterns that is driven on corresponding lanes. If AUTOINVSHPEN bit is set in port control register, the TXINVSHPFT field is rotated left at the completion of each pattern buffer set.

Function: 6 Offset:94h			
Bit	Attr	Default	Description
31:10	RV	000000h	Reserved
9:0	RWST	3FFh	TXINVSHPFT: Transmitter Inversion Shift Register.

**11.8.1.7 SBFIBRXSHFT: SB IBIST Receiver Inversion Shift Register**

Each bit in this register enables inverting the patterns that is received on corresponding lanes. If AUTOINVSHPEN bit is set in port control register, the RXINVSHPFT field is rotated left at the completion of each pattern buffer set.

Function: 6 Offset:98h			
Bit	Attr	Default	Description
31:10	RV	000000h	Reserved
9:0	RWST	3FFh	RXINVSHPFT: Receiver Inversion Shift Register.

**11.8.1.8 SBFIBRXLNERR: SB IBIST Receiver Lane Error Status**

This records the error status from each lane.

Function: 6 Offset:9Ch			
Bit	Attr	Default	Description
31:10	RV	000000h	Reserved
9:0	ROST	000h	RXERRSTAT: Receiver Error Status

**11.8.1.9 SBFIBPATTBUF2: SB IBIST Pattern Buffer 2 Register**

This register contains the pattern bits used in IBIST operations. Only the least significant 24 bits are used.

Function: 6 Offset:A0h			
Bit	Attr	Default	Description
31:24	RV	00h	Reserved
23:0	RWST	fd3302h	IBPATBUF2: IBIST Pattern Buffer 2 Pattern buffer storing the default and the user programmable pattern. Default: fd3302h

**11.8.1.10 SBFIBPATT2EN: SB IBIST Pattern Buffer 2 Enable**

This specifies which lanes will carry the pattern specified in SBFIBPATTBUFF2.

Function: 6 Offset:A4h			
Bit	Attr	Default	Description
31:10	RV	00h	Reserved
9:0	RWST	000h	SBFIBPATT2EN: IBIST Pattern Buffer 2 enable Per lane enable for driving pattern buffer 2.

**11.8.1.11 SBFIBINIT: SB IBIST Initialization Register**

This register control southbound IBIST Testing.

<b>Function: 6 Offset: B0h</b>			
<b>Bit</b>	<b>Attr</b>	<b>Default</b>	<b>Description</b>
31	RV	0	Reserved
30:21	RWST	0c8h	SBTS0CNT: Southbound TS0 Count Number of TS0 sequences to transmit.
20:13	RWST	01h	SBTS1CNT: Southbound TS1 Count Number of TS1 sequences to transmit.
12:3	RWST	100h	SBDISCNT: Southbound Disable State Count Number of cycles to remain in disable state.
2	RWST	1	SBCALIBEN: Southbound Calibration Enable 1 - Perform FBD Calibration.
1	RV	0	Reserved
0	RWST	0	SBIBISTINITEN: IBIST Initialization Enable 1 - Start IBIST Testing with Southbound Transmitter as the host.

**11.8.1.12 SBIBISTMISC: SB IBIST Initialization Miscellaneous Register**

This register control southbound IBIST Testing.

<b>Function: 6 Offset: B4h</b>			
<b>Bit</b>	<b>Attr</b>	<b>Default</b>	<b>Description</b>
31:24	RV	00h	Reserved
23:20	RWST	0h	AMBID: Value of the AMB ID field during TS0
19:0	RWST	61a80h	SBIBISTCALPERIOD: Number of cycles to drive 1 during Calibration



## 11.8.2 Northbound FBD IBIST registers

### 11.8.2.1 NBFIBPORTCTL: Northbound FBD IBIST Port Control Register

This register controls the operation of the IBIST logic.

**Northbound FBD IBIST Port Control Register Table**

Function: 6 Offset: C0h			
Bit	Attr	Default	Description
31:24	RV	00h	Reserved
23	RWST	0	SBNBMAP: Loopback mapping bit This bit will be sent during TS1 to specify to the target which lanes needs to be looped back. Actual lanes looped back is specified in the FBD Architecture Spec.
22	RWST	0	CMMSTR: Compliance Measurement Mode start This puts the IBIST logic in CMM mode and IBIST TX engine will start transmitting IBIST patterns.
21:12	RWCST	000h	ERRCNT: Error Counter Total number of errors encountered in this port.
11:8	ROST	0h	ERRLNNUM: Error Lane Number This points to the first lane that encountered an error. If more than one lane reports an error in a cycle, the most significant lane number that reported the error will be logged.
7:6	RWCST	00	ERRSTAT: Port Error Status When IBIST is started, status goes to 01 until first start delimiter is received and then goes to 00 until the end or to 10 if an error occurs. 00: No error. 01: Did not receive first start delimiter. 10: Transmission error (first error). 11: Reserved
5	RWST	0	AUTOINVSHPEN: Auto Inversion sweep enable This bit enables the inversion shift register to continuously rotate the pattern in the FIBTXSHFT and FIBRXSHFT registers. 0: Disable Auto-inversion 1: Enable Auto-inversions
4	RWST	0	STOPONERR: Stop IBIST on Error 0: Do not stop on error, only update error counter 1: Stop on error
3	RWST	0	LOOPCON: Loop forever 0: No looping 1: Loop forever
2	RWCST	0	COMPLETE: IBIST done flag 0: Not done 1: Done

**Northbound FBD IBIST Port Control Register Table (Continued)**

Function: 6 Offset: C0h			
Bit	Attr	Default	Description
1	RWST	0	MSTRMD: Controller Mode Enable When this bit is set, during the next TS1 training set, IBIST will transmit patterns generated locally rather than looping back the incoming test data. 0: Disable Controller mode 1: Enable Controller mode
0	RWST	0	IBISTR: IBIST Start When set, IBIST starts transmitting after the TS1 header is recognized during the next link initialization sequence. and <b>MSTRMD</b> bit is set. This bit also enables the receive engine to start looking for the start delimiter during TS1 training set. This bit is reset when IBIST is done. The IBIST transmitter can be stopped by setting this bit to 0. 0: Stop IBIST transmitter 1: Start IBIST transmitter

**11.8.2.2 NBFIBPGCTL: NB IBIST Pattern Generator Control Register**

This register contains bits to control the operation of the IBIST pattern generator. All counts are in 24 bit increments.

**NB IBIST Pattern Generator Control Register Table**

Function: 6 Offset: C4h			
Bit	Attr	Default	Description
31:26	RWST	0Fh	OVRLOOPCNT: Overall Loop Count 0h: Reserved 1h-3Fh: Number of times to loop all the patterns.
25:21	RWST	00h	CNSTGENCNT: Constant Generator Loop Counter 00h: Disable constant generator output 01h: 1Fh The number of times the constant generator counter pattern should loop before going to the next component. Each count represents 24 bits of 1's or 0's.
20	RWST	0	CNSTGENSET: Constant Generator Setting 0: Generate 0 1: Generate 1
19:13	RWST	0Fh	MODLOOPCNT: Modulo-N Loop Counter Each count represents 24 bits of the pattern specified by <b>MODPERIOD</b> . 00h: Disable Pattern Output 01h: 7Fh The number of times the Pattern Buffer should loop before going to the next component.

**NB IBIST Pattern Generator Control Register Table (Continued)**

<b>Function: 6</b> <b>Offset: C4h</b>			
<b>Bit</b>	<b>Attr</b>	<b>Default</b>	<b>Description</b>
12:10	RWST	001b	MODPERIOD: Period of the Modulo-N counter Each encoding transmits a 24-bit pattern as specified below. All other encodings are reserved. 001: L/2 - 0101_0101_0101_0101_0101_0101 010: L/4 - 0011_0011_0011_0011_0011_0011 011: L/6 - 0001_1100_0111_0001_1100_0111 100: L/8 - 0000_1111_0000_1111_0000_1111 110: L/24 - 0000_0000_0000_1111_1111_1111
9:3	RWST	0Fh	PATTLOOPCNT: Pattern Buffer Loop Counter 00h: Disable Pattern Output 01h: 7Fh The number of times the Pattern Buffer ( <b>IBPATBUF</b> ) should be repeated before going to the next component.
2:0	RWST	000	PTGENORD: Pattern Generation Order 000: Pattern Store + Modulo N Cntr + Constant Generator 001: Pattern Store + Constant Generator + Modulo N Cntr 010: Modulo N Cntr + Pattern Store + Constant Generator 011: Modulo N Cntr + Constant Generator + Pattern Store 100: Constant Generator + Pattern Store + Modulo N Cntr 101: Constant Generator + Modulo N Cntr + Pattern Store 110: Reserved 111: Reserved

**11.8.2.3 NBFIBPATBUF1: NB IBIST Pattern Buffer 1 Register**

This register contains the pattern bits used in IBIST operations. Only the least significant 24 bits are used.

<b>Function: 6</b> <b>Offset: C8h</b>			
<b>Bit</b>	<b>Attr</b>	<b>Default</b>	<b>Description</b>
31:24	RV	00h	Reserved
23:0	RWST	02ccfdh	IBPATBUF: IBIST Pattern Buffer Pattern buffer storing the default and the user programmable pattern.

#### 11.8.2.4 NBFIBTXMSK: NB IBIST Transmitter Mask Register

This register enables IBIST operations for individual lanes. This mask only applies to transmitters and not receivers.

Function: 6 Offset:CCh			
Bit	Attr	Default	Description
31:14	RV	00000h	Reserved
13:0	RWST	3FFFh	TXMASK: Selects which channels to enable for testing.

#### 11.8.2.5 NBFIBRXMSK: NB IBIST Receiver Mask Register

This register enables IBIST operations for individual lanes. This mask only applies to receivers and not transmitters.

Function: 6 Offset:D0h			
Bit	Attr	Default	Description
31:14	RV	00000h	Reserved
13:0	RWST	3FFFh	RXMASK: Selects which channels to enable for testing.

#### 11.8.2.6 NBFIBTXSHFT: NB IBIST Transmitter Inversion Shift Register

Each bit in this register enables inverting the patterns that is driven on corresponding lanes. If AUTOINVSHPEN bit is set in port control register, the TXINVSHFT field is rotated left at the completion of each pattern buffer set.

Function: 6 Offset:D4h			
Bit	Attr	Default	Description
31:14	RV	00000h	Reserved
13:0	RWST	3FFFh	TXINVSHFT: Transmitter Inversion Shift Register.

#### 11.8.2.7 NBFIBRXSHFT: NB IBIST Receiver Inversion Shift Register

Each bit in this register enables inverting the patterns that is received on corresponding lanes. If AUTOINVSHPEN bit is set in port control register, the RXINVSHFT field is rotated left at the completion of each pattern buffer set.

Function: 6 Offset:D8h			
Bit	Attr	Default	Description
31:14	RV	00000h	Reserved
13:0	RWST	3FFFh	RXINVSHFT: Receiver Inversion Shift Register.

**11.8.2.8 NBFIBRXLNERR: NB IBIST Receiver Lane Error Status**

This records the error status from each lane.

Function: 6 Offset:DCh			
Bit	Attr	Default	Description
31:14	RV	00000h	Reserved
13:0	ROST	0000h	RXERRSTAT: Receiver Error Status

**11.8.2.9 NBFIBPATTBUF2: NB IBIST Pattern Buffer 2 Register**

This register contains the pattern bits used in IBIST operations. Only the least significant 24 bits are used.

Function: 6 Offset:E0h			
Bit	Attr	Default	Description
31:24	RV	00h	Reserved
23:0	RWST	fd3302h	IBPATBUF2: IBIST Pattern Buffer 2 Pattern buffer storing the default and the user programmable pattern.

**11.8.2.10 NBFIBPATT2EN: NB IBIST Pattern Buffer 2 Enable**

This specifies which lanes will carry the pattern specified in NBFIBPATTBUFF2.

Function: 6 Offset:E4h			
Bit	Attr	Default	Description
15:14	RV	00	Reserved
13:0	RWST	0000h	IBPATBUF2EN: IBIST Pattern Buffer 2 enable Per lane enable for driving pattern buffer 2.

**11.8.2.11 NBFIBINIT: NB IBIST Initialization Register**

This register control northbound IBIST Testing.

<b>Function: 6</b> <b>Offset:F0h</b>			
<b>Bit</b>	<b>Attr</b>	<b>Default</b>	<b>Description</b>
31	RWST	0	SBIDLE: SB Link is not active This is to enable the NB link to complete training when there is no activity on the SB side. Normally NB waits for SB init to complete before proceeding with its training. 0 - Wait for SB 1 - Do not wait for SB
30:21	RWST	0c8h	NBTS0CNT: Northbound TS0 Count Number of TS0 sequences to transmit.
20:13	RWST	01h	NBTS1CNT: Northbound TS1 Count Number of TS1 sequences to transmit.
12:3	RWST	100h	NBDISCNT: Northbound Disable State Count Number of cycles to remain in disable state.
2	RWST	1	NBCALIBEN: Northbound Calibrating Enable 1 - Perform FBD Calibration.
1	RV	0	Reserved
0	RWST	0	NBIBISTINITEN: IBIST Initialization Enable 1 - Start IBIST Testing with Northbound Transmitter as the host.

**11.8.2.12 NBIBISTMISC: NB IBIST Initialization Miscellaneous Register**

This register control northbound IBIST Testing.

<b>Function: 6</b> <b>Offset:F4h</b>			
<b>Bit</b>	<b>Attr</b>	<b>Default</b>	<b>Description</b>
31:24	RV	0h	Reserved
23:20	RWST	0h	AMBID: Value of the AMB ID field during TS0
19:0	RWST	61a80h	NBIBISTCALPERIOD: Number of cycles to drive 1 during Calibration

## 12 Ballout and Package Information

### 12.1 655-ball FBGA (23x29 Array, 19.5x24.5 mm Body Size, 0.80 mm Pitch, MO-261A Variation AA/BA) Pin Configuration

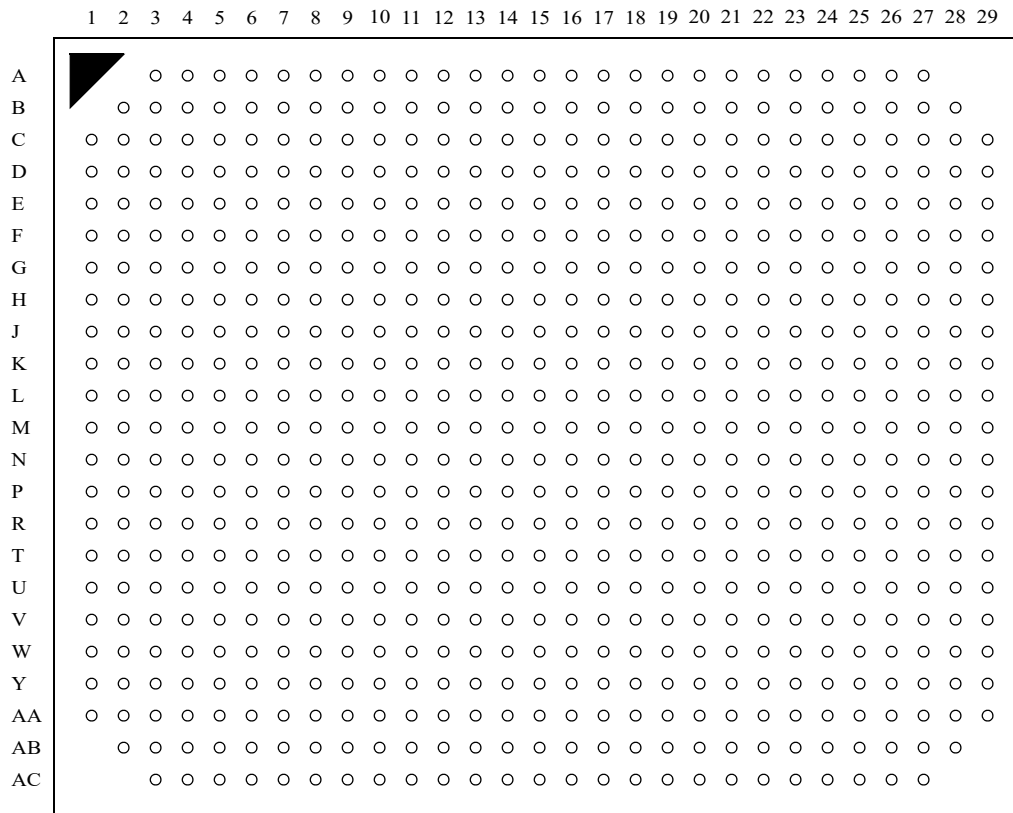


Figure 25 — Pinout Configuration

## 12.2 Pin Assignments for the Advanced Memory Buffer (AMB)

**Table 48 — 655-Ball FBGA (23x29 Array, 19.5x24.5 mm Body Size, 0.80 mm Pitch, MO-261A Variation AA/BA) - Left Side**

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A			V <sub>SS</sub>	DQ26	DQ12	V <sub>DD</sub>	DQS10	DQ13	V <sub>DD</sub>	$\overline{\text{DQS}}1$	DQ10	V <sub>DD</sub>	TESTLO	V <sub>DD</sub>	V <sub>DD</sub>
B		V <sub>DD</sub>	DQS3	$\overline{\text{DQS}}3$	V <sub>SS</sub>	DQ14	$\overline{\text{DQS}}10$	V <sub>SS</sub>	DQ11	DQS1	V <sub>SS</sub>	DDRC	TESTLO	V <sub>DD</sub>	V <sub>SS</sub>
C	V <sub>SS</sub>	DQS2	DQ18	V <sub>SS</sub>	DQ4	$\overline{\text{DQS}}9$	V <sub>SS</sub>	DQ15	DQ9	V <sub>SS</sub>	DQ8	DDRC	V <sub>SS</sub>	DDRC	DQS17
D	DQ19	$\overline{\text{DQS}}2$	V <sub>SS</sub>	DQ16	DQ24	V <sub>SS</sub>	DQS9	DQ7	V <sub>SS</sub>	DQ3	DQS0	V <sub>SS</sub>	$\overline{\text{DQS}}8$	DQS8	V <sub>DD</sub>
E	DQ21	V <sub>SS</sub>	DQ17	DQ29	V <sub>SS</sub>	DQ25	DQ6	V <sub>SS</sub>	DQ5	DQ1	V <sub>SS</sub>	DQ0	CB1	V <sub>SS</sub>	CB2
F	V <sub>SS</sub>	DQ20	DQ23	V <sub>SS</sub>	DQ31	DQ27	V <sub>SS</sub>	TESTLO	TEST	V <sub>SS</sub>	$\overline{\text{DQS}}0$	DQ2	V <sub>DD</sub>	CB0	CB3
G	$\overline{\text{DQS}}11$	DQS11	NC	NC	NC	V <sub>SS</sub>	DQS12	$\overline{\text{DQS}}12$	NC	NC	NC	BFUNC	RFU	RFU	RFU
H	DQ22	V <sub>SS</sub>	NC	NC	NC	DQ28	DQ30	V <sub>SS</sub>	NC	NC	NC	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>
J	V <sub>SS</sub>	CLK2	NC	NC	NC	BA1A	V <sub>SS</sub>	CKE1A	NC	NC	NC	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>
K	$\overline{\text{CLK}}2$	CLK0	NC	NC	NC	V <sub>SS</sub>	$\overline{\text{WE}}A$	$\overline{\text{RA}}SA$	NC	NC	NC	V <sub>SS</sub>	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>CC</sub>
L	$\overline{\text{CLK}}0$	V <sub>SS</sub>	NC	NC	NC	A0A	CKE0A	V <sub>SS</sub>	NC	NC	NC	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>CC</sub>	V <sub>SS</sub>
M	ODT0A	RFU	NC	NC	NC	$\overline{\text{CA}}SA$	V <sub>SS</sub>	BA2A	NC	NC	NC	V <sub>SS</sub>	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>CC</sub>
N	$\overline{\text{CS}}1A$	$\overline{\text{CS}}0A$	NC	NC	NC	V <sub>SS</sub>	BA0A	A10A	NC	NC	NC	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>CC</sub>	V <sub>SS</sub>
P	A6A	V <sub>SS</sub>	NC	NC	NC	A2A	A1A	A3A	NC	NC	NC	V <sub>SS</sub>	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>CC</sub>
R	V <sub>SS</sub>	A8A	NC	NC	NC	A11A	V <sub>SS</sub>	A5A	NC	NC	NC	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>CC</sub>	V <sub>SS</sub>
T	A4A	A13A	NC	NC	NC	V <sub>SS</sub>	A9A	A7A	NC	NC	NC	V <sub>SS</sub>	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>CC</sub>
U	PN0	$\overline{\text{PN}}0$	NC	NC	NC	A15A	A14A	A12A	NC	NC	NC	RFU	V <sub>CCFBD</sub>	V <sub>SS</sub>	V <sub>SS</sub>
V	PN1	$\overline{\text{PN}}1$	V <sub>SS</sub>	SN0	$\overline{\text{SN}}0$	V <sub>CCFBD</sub>	V <sub>SS</sub>	V <sub>CCFBD</sub>	V <sub>SS</sub>	RFU <sup>1</sup>	RFU <sup>1</sup>	V <sub>CCFBD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>
W	PN2	$\overline{\text{PN}}2$	V <sub>SS</sub>	SN1	$\overline{\text{SN}}1$	$\overline{\text{SN}}3$	$\overline{\text{SN}}4$	$\overline{\text{SN}}5$	$\overline{\text{SN}}13$	$\overline{\text{SN}}12$	$\overline{\text{SN}}6$	$\overline{\text{SN}}7$	$\overline{\text{SN}}8$	$\overline{\text{SN}}9$	$\overline{\text{SN}}10$
Y	PN3	$\overline{\text{PN}}3$	V <sub>SS</sub>	SN2	$\overline{\text{SN}}2$	SN3	SN4	SN5	SN13	SN12	SN6	SN7	SN8	SN9	SN10
AA	V <sub>SS</sub>	PN4	$\overline{\text{PN}}4$	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>
AB		V <sub>SS</sub>	RESET	PN5	PN13	RFU <sup>1</sup>	PN12	PN6	PN7	PN8	PN9	V <sub>SSAPLL</sub>	V <sub>CCAPLL</sub>	PN10	PN11
AC			V <sub>SS</sub>	PN5	PN13	RFU <sup>1</sup>	PN12	PN6	PN7	PN8	PN9	FBDRES	PLLTSTO	PN10	PN11

NOTE 1 These pin positions are reserved for forward clocks to be used in future AMB implementations.



## 12.2 Pin Assignments for the Advanced Memory Buffer (AMB) (cont'd)

**Table 49 — 655-Ball FBGA (23x29 Array, 19.5x24.5 mm Body Size, 0.80 mm Pitch, MO-261A Variation AA/BA) - Right Side**

	16	17	18	19	20	21	22	23	24	25	26	27	28	29
A	V <sub>DD</sub>	TEST	V <sub>DD</sub>	DQ52	DQS15	V <sub>DD</sub>	DQ49	$\overline{\text{DQS6}}$	V <sub>DD</sub>	DQ48	DQ38	V <sub>DD</sub>		
B	V <sub>DD</sub>	TESTLO	DDRC	V <sub>SS</sub>	$\overline{\text{DQS15}}$	DQ53	V <sub>SS</sub>	DQS6	DQ50	V <sub>SS</sub>	$\overline{\text{DQS13}}$	DQS13	V <sub>SS</sub>	
C	$\overline{\text{DQS17}}$	V <sub>SS</sub>	DDRC	DQ54	V <sub>SS</sub>	DQ55	DQ51	V <sub>SS</sub>	DQS7	DQ56	V <sub>SS</sub>	DQ46	$\overline{\text{DQS14}}$	V <sub>DD</sub>
D	CB6	CB7	V <sub>SS</sub>	DQS16	DQ63	V <sub>SS</sub>	DQ59	$\overline{\text{DQS7}}$	V <sub>SS</sub>	DQ36	DQ44	V <sub>SS</sub>	DQS14	DQ47
E	V <sub>SS</sub>	CB5	$\overline{\text{DQS16}}$	V <sub>SS</sub>	DQ61	DQ57	V <sub>SS</sub>	DQ58	DQ39	V <sub>SS</sub>	DQ33	DQ45	V <sub>SS</sub>	DQ41
F	CB4	V <sub>DD</sub>	DQ62	DQ60	V <sub>SS</sub>	TEST	TEST	V <sub>SS</sub>	DQ37	DQ35	V <sub>SS</sub>	$\overline{\text{DQS5}}$	DQ43	V <sub>SS</sub>
G	TESTLO	RFU	RFU	NC	NC	NC	DQS4	$\overline{\text{DQS4}}$	V <sub>SS</sub>	NC	NC	NC	DQS5	DQ40
H	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	NC	NC	NC	V <sub>SS</sub>	DQ34	DQ32	NC	NC	NC	V <sub>SS</sub>	DQ42
J	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	NC	NC	NC	$\overline{\text{RASB}}$	V <sub>SS</sub>	RFU	NC	NC	NC	$\overline{\text{CLK3}}$	V <sub>SS</sub>
K	V <sub>SS</sub>	V <sub>CC</sub>	V <sub>SS</sub>	NC	NC	NC	ODT0B	$\overline{\text{CS1B}}$	V <sub>SS</sub>	NC	NC	NC	$\overline{\text{CLK1}}$	CLK3
L	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>CC</sub>	NC	NC	NC	V <sub>SS</sub>	$\overline{\text{CASB}}$	$\overline{\text{WEB}}$	NC	NC	NC	V <sub>SS</sub>	CLK1
M	V <sub>SS</sub>	V <sub>CC</sub>	V <sub>SS</sub>	NC	NC	NC	$\overline{\text{CS0B}}$	V <sub>SS</sub>	BA1B	NC	NC	NC	CKE0B	V <sub>SS</sub>
N	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>CC</sub>	NC	NC	NC	A0B	A2B	V <sub>SS</sub>	NC	NC	NC	BA0B	BA2B
P	V <sub>SS</sub>	V <sub>CC</sub>	V <sub>SS</sub>	NC	NC	NC	V <sub>SS</sub>	A4B	A1B	NC	NC	NC	V <sub>SS</sub>	CKE1B
R	V <sub>CC</sub>	V <sub>SS</sub>	V <sub>CC</sub>	NC	NC	NC	A6B	V <sub>SS</sub>	A10B	NC	NC	NC	A3B	V <sub>SS</sub>
T	V <sub>SS</sub>	V <sub>CC</sub>	V <sub>SS</sub>	NC	NC	NC	A11B	A9B	V <sub>SS</sub>	NC	NC	NC	A7B	A5B
U	V <sub>SS</sub>	V <sub>CCFBD</sub>	RFU	NC	NC	NC	A8B	A15B	A14B	SA0	SCL	SDA	$\overline{\text{PS8}}$	PS8
V	V <sub>CCFBD</sub>	V <sub>SS</sub>	V <sub>CCFBD</sub>	V <sub>SS</sub>	V <sub>CCFBD</sub>	RFU <sup>1</sup>	RFU <sup>1</sup>	V <sub>SS</sub>	A13B	A12 B	SA2	SA1	$\overline{\text{PS7}}$	PS7
W	V <sub>SS</sub>	$\overline{\text{SS0}}$	$\overline{\text{SS1}}$	$\overline{\text{SS2}}$	$\overline{\text{SS3}}$	$\overline{\text{SS4}}$	$\overline{\text{SS9}}$	$\overline{\text{SS5}}$	$\overline{\text{SS6}}$	$\overline{\text{SS7}}$	$\overline{\text{SS8}}$	V <sub>SS</sub>	$\overline{\text{PS6}}$	PS6
Y	V <sub>SS</sub>	SS0	SS1	SS2	SS3	SS4	SS9	SS5	SS6	SS7	SS8	V <sub>SS</sub>	$\overline{\text{PS5}}$	PS5
AA	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	$\overline{\text{PS9}}$	PS9
AB	V <sub>SS</sub>	$\overline{\text{SN11}}$	V <sub>SS</sub>	SCK	TESTLO _AB20	$\overline{\text{PS0}}$	$\overline{\text{PS1}}$	$\overline{\text{PS2}}$	$\overline{\text{PS3}}$	$\overline{\text{PS4}}$	RFU <sup>1</sup>	V <sub>DDSPD</sub>	V <sub>SS</sub>	
AC	RFU	SN11	V <sub>SS</sub>	$\overline{\text{SCK}}$	TESTLO _AC20	PS0	PS1	PS2	PS3	PS4	RFU <sup>1</sup>	V <sub>SS</sub>		

NOTE 1 These pin positions are reserved for forward clocks to be used in future AMB implementations.

**12.2 Pin Assignments for the Advanced Memory Buffer (AMB) (cont'd)****Table 50 — Advanced Memory Buffer Signals By Ball Number**

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
A3	VSS	B15	VSS	C25	DQ56
A4	DQ26	B16	VDD	C26	VSS
A5	DQ12	B17	TESTLO	C27	DQ46
A6	VDD	B18	DDRC_B18	C28	$\overline{\text{DQS}}14$
A7	DQS10	B19	VSS	C29	VDD
A8	DQ13	B20	$\overline{\text{DQS}}15$	D1	DQ19
A9	VDD	B21	DQ53	D2	$\overline{\text{DQS}}2$
A10	$\overline{\text{DQS}}1$	B22	VSS	D3	VSS
A11	DQ10	B23	DQS6	D4	DQ16
A12	VDD	B24	DQ50	D5	DQ24
A13	TESTLO	B25	VSS	D6	VSS
A14	VDD	B26	$\overline{\text{DQS}}13$	D7	DQS9
A15	VDD	B27	DQS13	D8	DQ7
A16	VDD	B28	VSS	D9	VSS
A17	TEST	C1	VSS	D10	DQ3
A18	VDD	C2	DQS2	D11	DQS0
A19	DQ52	C3	DQ18	D12	VSS
A20	DQS15	C4	VSS	D13	$\overline{\text{DQS}}8$
A21	VDD	C5	DQ4	D14	DQS8
A22	DQ49	C6	$\overline{\text{DQS}}9$	D15	VDD
A23	$\overline{\text{DQS}}6$	C7	VSS	D16	CB6
A24	VDD	C8	DQ15	D17	CB7
A25	DQ48	C9	DQ9	D18	VSS
A26	DQ38	C10	VSS	D19	DQS16
A27	VDD	C11	DQ8	D20	DQ63
B2	VDD	C12	DDRC_C12	D21	VSS
B3	DQS3	C13	VSS	D22	DQ59
B4	$\overline{\text{DQS}}3$	C14	DDRC_C14	D23	$\overline{\text{DQS}}7$
B5	VSS	C15	DQS17	D24	VSS
B6	DQ14	C16	$\overline{\text{DQS}}17$	D25	DQ36
B7	$\overline{\text{DQS}}10$	C17	VSS	D26	DQ44
B8	VSS	C18	DDRC_C18	D27	VSS
B9	DQ11	C19	DQ54	D28	DQS14
B10	DQS1	C20	VSS	D29	DQ47
B11	VSS	C21	DQ55	E1	DQ21
B12	DDRC_B12	C22	DQ51	E2	VSS
B13	TESTLO	C23	VSS	E3	DQ17
B14	VDD	C24	DQS7	E4	DQ29

**Table 50 — Advanced Memory Buffer Signals By Ball Number (Continued)**

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
E5	VSS	F14	CB0	G23	$\overline{\text{DQS}}4$
E6	DQ25	F15	CB3	G24	VSS
E7	DQ6	F16	CB4	G25	NC
E8	VSS	F17	VDD	G26	NC
E9	DQ5	F18	DQ62	G27	NC
E10	DQ1	F19	DQ60	G28	DQS5
E11	VSS	F20	VSS	G29	DQ40
E12	DQ0	F21	TEST	H1	DQ22
E13	CB1	F22	TEST	H2	VSS
E14	VSS	F23	VSS	H3	NC
E15	CB2	F24	DQ37	H4	NC
E16	VSS	F25	DQ35	H5	NC
E17	CB5	F26	VSS	H6	DQ28
E18	$\overline{\text{DQS}}16$	F27	$\overline{\text{DQS}}5$	H7	DQ30
E19	VSS	F28	DQ43	H8	VSS
E20	DQ61	F29	VSS	H9	NC
E21	DQ57	G1	$\overline{\text{DQS}}11$	H10	NC
E22	VSS	G2	DQS11	H11	NC
E23	DQ58	G3	NC	H12	VSS
E24	DQ39	G4	NC	H13	VDD
E25	VSS	G5	NC	H14	VSS
E26	DQ33	G6	VSS	H15	VDD
E27	DQ45	G7	DQS12	H16	VSS
E28	VSS	G8	$\overline{\text{DQS}}12$	H17	VDD
E29	DQ41	G9	NC	H18	VSS
F1	VSS	G10	NC	H19	NC
F2	DQ20	G11	NC	H20	NC
F3	DQ23	G12	BFUNC	H21	NC
F4	VSS	G13	RFU	H22	VSS
F5	DQ31	G14	RFU	H23	DQ34
F6	DQ27	G15	RFU	H24	DQ32
F7	VSS	G16	TESTLO	H25	NC
F8	TESTLO	G17	RFU	H26	NC
F9	TEST	G18	RFU	H27	NC
F10	VSS	G19	NC	H28	VSS
F11	$\overline{\text{DQS}}0$	G20	NC	H29	DQ42
F12	DQ2	G21	NC	J1	VSS
F13	VDD	G22	DQS4	J2	CLK2

**Table 50 — Advanced Memory Buffer Signals By Ball Number (Continued)**

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
J3	NC	K12	VSS	L21	NC
J4	NC	K13	VCC	L22	VSS
J5	NC	K14	VSS	L23	CASB
J6	BA1A	K15	VCC	L24	WEB
J7	VSS	K16	VSS	L25	NC
J8	CKE1A	K17	VCC	L26	NC
J9	NC	K18	VSS	L27	NC
J10	NC	K19	NC	L28	VSS
J11	NC	K20	NC	L29	CLK1
J12	VDD	K21	NC	M1	ODT0A
J13	VSS	K22	ODT0B	M2	RFU
J14	VDD	K23	CS1B	M3	NC
J15	VSS	K24	VSS	M4	NC
J16	VDD	K25	NC	M5	NC
J17	VSS	K26	NC	M6	CASA
J18	VDD	K27	NC	M7	VSS
J19	NC	K28	CLK1	M8	BA2A
J20	NC	K29	CLK3	M9	NC
J21	NC	L1	CLK0	M10	NC
J22	RASB	L2	VSS	M11	NC
J23	VSS	L3	NC	M12	VSS
J24	RFU	L4	NC	M13	VCC
J25	NC	L5	NC	M14	VSS
J26	NC	L6	A0A	M15	VCC
J27	NC	L7	CKE0A	M16	VSS
J28	CLK3	L8	VSS	M17	VCC
J29	VSS	L9	NC	M18	VSS
K1	CLK2	L10	NC	M19	NC
K2	CLK0	L11	NC	M20	NC
K3	NC	L12	VCC	M21	NC
K4	NC	L13	VSS	M22	CS0B
K5	NC	L14	VCC	M23	VSS
K6	VSS	L15	VSS	M24	BA1B
K7	WEA	L16	VCC	M25	NC
K8	RASA	L17	VSS	M26	NC
K9	NC	L18	VCC	M27	NC
K10	NC	L19	NC	M28	CKE0B
K11	NC	L20	NC	M29	VSS

**Table 50 — Advanced Memory Buffer Signals By Ball Number (Continued)**

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
N1	$\overline{CS1A}$	P10	NC	R19	NC
N2	$\overline{CS0A}$	P11	NC	R20	NC
N3	NC	P12	VSS	R21	NC
N4	NC	P13	VCC	R22	A6B
N5	NC	P14	VSS	R23	VSS
N6	VSS	P15	VCC	R24	A10B
N7	BA0A	P16	VSS	R25	NC
N8	A10A	P17	VCC	R26	NC
N9	NC	P18	VSS	R27	NC
N10	NC	P19	NC	R28	A3B
N11	NC	P20	NC	R29	VSS
N12	VCC	P21	NC	T1	A4A
N13	VSS	P22	VSS	T2	A13A
N14	VCC	P23	A4B	T3	NC
N15	VSS	P24	A1B	T4	NC
N16	VCC	P25	NC	T5	NC
N17	VSS	P26	NC	T6	VSS
N18	VCC	P27	NC	T7	A9A
N19	NC	P28	VSS	T8	A7A
N20	NC	P29	CKE1B	T9	NC
N21	NC	R1	VSS	T10	NC
N22	A0B	R2	A8A	T11	NC
N23	A2B	R3	NC	T12	VSS
N24	VSS	R4	NC	T13	VCC
N25	NC	R5	NC	T14	VSS
N26	NC	R6	A11A	T15	VCC
N27	NC	R7	VSS	T16	VSS
N28	BA0B	R8	A5A	T17	VCC
N29	BA2B	R9	NC	T18	VSS
P1	A6A	R10	NC	T19	NC
P2	VSS	R11	NC	T20	NC
P3	NC	R12	VCC	T21	NC
P4	NC	R13	VSS	T22	A11B
P5	NC	R14	VCC	T23	A9B
P6	A2A	R15	VSS	T24	VSS
P7	A1A	R16	VCC	T25	NC
P8	A3A	R17	VSS	T26	NC
P9	NC	R18	VCC	T27	NC

**Table 50 — Advanced Memory Buffer Signals By Ball Number (Continued)**

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
T28	A7B	V8	VCCFBD	W17	$\overline{SS}0$
T29	A5B	V9	VSS	W18	$\overline{SS}1$
U1	PN0	V10	RFU <sup>1</sup>	W19	$\overline{SS}2$
U2	$\overline{PN}0$	V11	RFU <sup>1</sup>	W20	$\overline{SS}3$
U3	NC	V12	VCCFBD	W21	$\overline{SS}4$
U4	NC	V13	VSS	W22	$\overline{SS}9$
U5	NC	V14	VSS	W23	$\overline{SS}5$
U6	A15A	V15	VSS	W24	$\overline{SS}6$
U7	A14A	V16	VCCFBD	W25	$\overline{SS}7$
U8	A12A	V17	VSS	W26	$\overline{SS}8$
U9	NC	V18	VCCFBD	W27	VSS
U10	NC	V19	VSS	W28	$\overline{PS}6$
U11	NC	V20	VCCFBD	W29	PS6
U12	RFU	V21	RFU <sup>1</sup>	Y1	PN3
U13	VCCFBD	V22	RFU <sup>1</sup>	Y2	$\overline{PN}3$
U14	VSS	V23	VSS	Y3	VSS
U15	VSS	V24	A13B	Y4	SN2
U16	VSS	V25	A12B	Y5	$\overline{SN}2$
U17	VCCFBD	V26	SA2	Y6	SN3
U18	RFU	V27	SA1	Y7	SN4
U19	NC	V28	$\overline{PS}7$	Y8	SN5
U20	NC	V29	PS7	Y9	SN13
U21	NC	W1	PN2	Y10	SN12
U22	A8B	W2	$\overline{PN}2$	Y11	SN6
U23	A15B	W3	VSS	Y12	SN7
U24	A14B	W4	SN1	Y13	SN8
U25	SA0	W5	$\overline{SN}1$	Y14	SN9
U26	SCL	W6	$\overline{SN}3$	Y15	SN10
U27	SDA	W7	$\overline{SN}4$	Y16	VSS
U28	$\overline{PS}8$	W8	$\overline{SN}5$	Y17	SS0
U29	PS8	W9	$\overline{SN}13$	Y18	SS1
V1	PN1	W10	$\overline{SN}12$	Y19	SS2
V2	$\overline{PN}1$	W11	$\overline{SN}6$	Y20	SS3
V3	VSS	W12	$\overline{SN}7$	Y21	SS4
V4	SN0	W13	$\overline{SN}8$	Y22	SS9
V5	$\overline{SN}0$	W14	$\overline{SN}9$	Y23	SS5
V6	VCCFBD	W15	$\overline{SN}10$	Y24	SS6
V7	VSS	W16	VSS	Y25	SS7
NOTE 1 These pin positions are reserved for forward clocks to be used in future AMB implementations.					

**Table 50 — Advanced Memory Buffer Signals By Ball Number (Continued)**

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
Y26	SS8	AB7	$\overline{\text{PN}}12$	AC19	$\overline{\text{SCK}}$
Y27	VSS	AB8	$\overline{\text{PN}}6$	AC20	TESTLO_AC20
Y28	$\overline{\text{PS}}5$	AB9	$\overline{\text{PN}}7$	AC21	PS0
Y29	PS5	AB10	$\overline{\text{PN}}8$	AC22	PS1
AA1	VSS	AB11	$\overline{\text{PN}}9$	AC23	PS2
AA2	PN4	AB12	VSSAPLL	AC24	PS3
AA3	$\overline{\text{PN}}4$	AB13	VCCAPLL	AC25	PS4
AA4	VSS	AB14	$\overline{\text{PN}}10$	AC26	RFU <sup>1</sup>
AA5	VSS	AB15	$\overline{\text{PN}}11$	AC27	VSS
AA6	VSS	AB16	VSS		
AA7	VSS	AB17	$\overline{\text{SN}}11$		
AA8	VSS	AB18	VSS		
AA9	VSS	AB19	SCK		
AA10	VSS	AB20	TESTLO_AB20		
AA11	VSS	AB21	$\overline{\text{PS}}0$		
AA12	VSS	AB22	$\overline{\text{PS}}1$		
AA13	VSS	AB23	$\overline{\text{PS}}2$		
AA14	VSS	AB24	$\overline{\text{PS}}3$		
AA15	VSS	AB25	$\overline{\text{PS}}4$		
AA16	VSS	AB26	RFU <sup>1</sup>		
AA17	VSS	AB27	VDDSPD		
AA18	VSS	AB28	VSS		
AA19	VSS	AC3	VSS		
AA20	VSS	AC4	PN5		
AA21	VSS	AC5	PN13		
AA22	VSS	AC6	RFU <sup>1</sup>		
AA23	VSS	AC7	PN12		
AA24	VSS	AC8	PN6		
AA25	VSS	AC9	PN7		
AA26	VSS	AC10	PN8		
AA27	$\overline{\text{PS}}9$	AC11	PN9		
AA28	PS9	AC12	FBDRES		
AA29	VSS	AC13	PLLTSTO		
AB2	VSS	AC14	PN10		
AB3	$\overline{\text{RESET}}$	AC15	PN11		
AB4	$\overline{\text{PN}}5$	AC16	RFU		
AB5	$\overline{\text{PN}}13$	AC17	SN11		
AB6	RFU <sup>1</sup>	AC18	VSS		
NOTE 1 These pin positions are reserved for forward clocks to be used in future AMB implementations.					

### 12.3 Package Information

Refer to Registered Outline MO-261A published by JC-11 committee for AMB package info.

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## 13 AMB Quad Rank Support

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### 13.1 Background

FB-DIMM supports 2 ranks per DIMM in the Architecture and Protocol spec, the AMB implementations, and the Host Controller designs.

This specification describes the implementation to achieve 4 ranks per DIMM. This is accomplished by making the DIMM appear to have the next higher density DRAMs installed, such that 2 ranks appear to the host controller as 1 rank. Quad Rank Mode A is also included in the AMB, allowing the host controller to utilize that mode of operation. The AMB must support both modes. The difference is in how the Rank Select 1 is determined.

### 13.2 AMB signal changes and DRAM connections

#### 13.2.1 Quad Rank Signal Requirements

Additional control signals (chip select and ODT) are required for quad rank operation. The Quad rank requirements are as follows:

**Table 51 — Function Mapping Legend**

Signal	Existing (SR and DR)	Quad Rank Requirement
Chip Select (CS#)	Two chip selects provided, with A and B copies.	Chip Selects are independent per rank, requiring 4 independently controlled Chip Selects. There are not separate A and B signals provided. One signal from the AMB drives both sides, and is terminated on each end.
ODT	One ODT provided, with A and B copies. Both ranks controlled by the one ODT signal.	The original ODT with A and B copies are maintained. Optionally, two more ODT signals are provided that are used for two new ranks. ODT usage is raw card dependent.
CKE	Two CKE signals provided, with A and B copies. AMB (and host) has individual control of CKE on each rank.	For raw cards that require 4 ODT signals, two CKE signals provided, but only the "A" copies, which drive both sides. For raw cards that require only 2 ODT signals, both the A and B copies of the CKE signals are available. CKE0 drives ranks 0 and 2, while CKE1 drives ranks 1 and 3. The AMB (and host) can control the CKE for rank pairs.
DRAM Address	A[15:0] provided with A and B copies.	A15 is not required, as 4 Gbit devices are not supported by this quad rank spec. They are reused as ECCA2 and ECCA6, which are separately controlled copies of A2 and A6 sent only to the ECC DRAMs. Normally they are exact copies of A2 and A6, but during MRS commands, can be controlled separately by the AMB via the DCALADDR register.



### 13.2.2 Address and Control Signal Reuse

The existing AMB address and control signals are re-used for quad rank by:

- Reassigning an address bit not required by 2Gbit and below DRAMs
- Providing only one copy of chip selects, rather than an "A" and "B" copy.
- Optionally providing only one copy of the CKE signals, rather than an "A" and "B" copy.

#### 13.2.2.1 Reassigning Address Bits

An AMB provides A0 through A15, and BA0 through BA2 signals to the DRAMs, but lower density DRAMs do not require all of these address signals. Specifically, A15 is not used until 4Gbit DRAMs which are not likely to be available in DDR2, and are not supported by this quad rank spec.

#### 13.2.2.2 One Copy of Chip Select and (Optionally) CKE Signals

The AMB has two copies of all DDR interface address, command, and control signals, one for the DRAMs on the left side of the DIMM and one for the DRAMs on the right side of the DIMM. These are labeled "A" and "B" at the end of the signal names. Each signal is terminated to Vtt via a resistor at the physical end of the DIMM.

For quad rank x8 DIMMs, the chip select signals are routed to only 9 DRAMs each, allowing one chip select signal to drive both sides for each rank. A dual termination scheme is used, providing a termination resistor on each end of the DIMM. Quad rank x4 would route each chip select and to 18 DRAMs each.

Optionally, the CKE0A and CKE1A signals also drive both the left and right sides for quad rank, with a dual termination scheme.

#### 13.2.2.3 ODT Requirements of Quad Rank

There are two options for the ODT signals for quad rank operation. Option 1 provides two additional ODT signals that are used for ranks 2 and 3. Option 2 uses only the two original ODT signals.

In both cases, the ODT for the rank 0 and 1 DRAMs are identical for quad rank as for single and dual rank DIMMs with 2 physical copies provided (ODT0A and ODT0B) to minimize the loading and/or simplify the routing.

In option 1, ranks 2 and 3 are controlled by the two new ODT signals, ODT1 and ODT2 respectively. This scheme requires a total of 4 ODT pins.

The ODT functionality is programmable, and it will depend on particular DIMM implementation.

Note that the functionality of original ODTA/B signals for rank 0 and rank 1 is completely unchanged, including the register programming.

#### 13.2.2.4 ECCA2 and ECCA6

The signal routing topology of the ECC DRAMs may require different strength of ODT on the ECC DRAMs from the data DRAMs. The ODT strength is programmed through MRS commands, which will program all DRAMs of a rank with the same value via the DRAM address bus. The ODT strength is programmed via EMRS1 bits A6 and A2.

To allow the ECC DRAMs to have their ODT strength programmed separately, the AMB creates a separate A2 and A6 for the ECC DRAMs. These signals normally follow the A2 and A6 functionality, but on all MRS cycles, AMB can send out separate values.

ECCA2 and ECCA6 are connected to all 4 rank's ECC bits. ECCA2 and ECCA6 are non-inverted outputs when address inversion is enabled.

### 13.2.3 Quad Rank Signal Mapping

Table 52 and Table 53 show the mapping of the chip select, ODT, and CKE signals to each rank. The Signal name is the logical signal. The mapping to physical AMB balls is listed in a follow on table.

**Table 52 — Quad Rank Signal Mapping per Rank, ODT Option 1**

Signal	Rank0	Rank1	Rank2	Rank3
CS0#	CS			
CS1#		CS		
CS2#			CS	
CS3#				CS
ODTA		ODT		
ODTB	ODT			
ODT1			ODT	
ODT2				ODT
CKE0	CKE		CKE	
CKE1		CKE		CKE

**Table 53 — Quad Rank Signal Mapping per Rank, ODT Option 2**

Signal	Rank0	Rank1	Rank2	Rank3
CS0#	CS			
CS1#		CS		
CS2#			CS	
CS3#				CS
ODT0A/B <sup>a</sup>	ODT	ODT		
VSS			ODT	ODT
CKE0A/B <sup>1</sup>	CKE		CKE	
CKE1A/B <sup>1</sup>		CKE		CKE
NOTE a For ODT Option 2, CKE and ODT A and B copies are routed to the left and right sides of the DIMM in the same manner as dual rank DIMMs				

### 13.2.4 Mapping to AMB Balls

Table 54 shows the mapping between the existing AMB balls and the quad rank signals.

**Table 54 — AMB Pin Usage for each DIMM Type**

AMB Ball	Non-QR (SR or DR)	Quad Rank ODT Opt 1	Quad Rank ODT Opt 2	Quad Rank Comment
CS0#A	CS0#A	CS0# <sup>a</sup>	CS0# <sup>1</sup>	Rank 0
CS0#B	CS0#B	CS2# <sup>1</sup>	CS2# <sup>1</sup>	Rank 1
CS1#A	CS1#A	CS1# <sup>1</sup>	CS1# <sup>1</sup>	Rank 2
CS1#B	CS1#B	CS3# <sup>1</sup>	CS3# <sup>1</sup>	Rank 3
ODTA	ODTA	ODTA <sup>b</sup>	ODTA <sup>2</sup>	First ODT
ODTB	ODTB	ODTB <sup>2</sup>	ODTB <sup>2</sup>	Second ODT
A15A	A15A	ECCA2	ECCA2	A2 for the ECC DRAMs
A15B	A15B	ECCA6	ECCA6	A6 for the ECC DRAMs
CKE0A	CKE0A	CKE0	CKE0A	Ranks 0 and 2
CKE0B	CKE0B	ODT1	CKE0B	Optional third ODT, or CKE0B for Ranks 0 and 2
CKE1A	CKE1A	CKE1	CKE1A	Ranks 1 and 3
CKE1B	CKE1B	ODT2	CKE1B	Optional third ODT, or CKE1B for Ranks 1 and 3
NOTE a There are no separate A and B copies for the CS# signals in Quad Rank				
NOTE b Logically identical				

### 13.2.5 Signal State at Reset

CKE and ODT signals must be low during the DRAM power ramp. Since CKE signals are muxed with ODT signals, there is no power up difference. On a quad rank DIMM, the BIOS should set the register bit to configure the CKE0B and CKE1B signals to the ODT functionality (if applicable) prior to taking CKE high.

## 13.3 Rank Decode

FBD Quad Rank allows two addressing modes for the additional ranks. The AMB must implement both modes. The host may choose which mode to implement.

Mode C is specific to FBD and uses a bank or row address bit as the additional rank select bit. This mode allows for the full 8 DIMMs per channel. This mode appears to the host controller as a dual rank DIMM.

Mode A uses DS2 as the additional rank select bit. It limits the number of DIMMs per channel to 4 when quad rank is being used.

### 13.3.1 Quad Rank Mode C

Quad rank mode C operates by making two physical ranks show up as one logical rank. A bank address bit as well as the existing RS bit determines which rank the AMB will access. The host controller will see the DIMM as dual rank, with each rank being one density higher than the physical DRAMs.

### 13.3.1 Quad Rank Mode C (cont'd)

The host controller sends one Rank Select bit with the DRAM commands that are rank specific. This is called RS in the FBD spec, and will be called RS0 here. The AMB must create an RS1 bit internally to determine which of the 4 ranks to access. RS1 will be used to divide each logical rank into 2 physical ranks on the DIMM. Logical Rank 0 will be divided into physical ranks 0 and 2, while Logical Rank 1 will be divided into physical ranks 1 and 3.

**Table 55 — RS1:0 to Rank Decode**

<b>RS1 (created inside the AMB from BA0)</b>	<b>RS0 (RS field in FBD commands)</b>	<b>Rank Accessed</b>
0	0	0
0	1	1
1	0	2
1	1	3

In the AMB the BA0 bit from the host controller is used to create RS1. This places the even numbered banks in one physical rank, and the odd numbered banks in the other physical rank.

The AMB must recreate the BA0 signal to the DRAMs (called dBA0 here), which is done differently depending on the DRAM density.

**Table 56 — dBA0 (DRAM BA0) Selection by DRAM Density**

<b>DRAM Density</b>	<b>dBA0 (DRAM BA0) bit:</b>
512 Mbit	Host BA2
1 Gbit	Host Row A14
2 Gbit	Host Row A15

Table 57 shows the physical layout of each DRAM type, and how the host controller will view the DIMM.

**Table 57 — DIMM Addressing**

<b>Physical x8 DRAMs on DIMM</b>					<b>Host Controller View</b>				
<b>Rank</b>	<b>Density</b>	<b>Banks</b>	<b>Row Bits</b>	<b>Col Bits</b>	<b>Rank</b>	<b>Density</b>	<b>Banks</b>	<b>Row Bits</b>	<b>Col Bits</b>
4	512 Mbit	4	14	10	2	1 Gbit	<b>8</b>	14	10
4	1 Gbit	8	14	10	2	2 Gbit	8	<b>15</b>	10
4	2 Gbit*	8	15	10	2	4 Gbit	8	<b>16</b>	10

\* Some QR DIMMs may not support 2Gbit DRAMs

**512 Mbit** QR DIMMs appear to the host controller logically as Dual Rank 1Gbit DIMMs. The difference between 512 Mbit parts and 1Gbit parts is the addition of BA2 (Bank Address 2) for both row and column commands. The AMB will use BA2 in the FBD command as dBA0 to the DRAMs. Note that BA2 is sent on both row and column commands to the DRAMs so this is a simple mapping.

### 13.3.1 Quad Rank Mode C (cont'd)

**1 Gbit** QR DIMMs appear to the host controller logically as Dual Rank 2 Gbit DIMMs. The difference between a 1 Gbit part and 2 Gbit parts is the addition of A14 for the Activate Command. The AMB will use Row address A14 in the FBD command as dBA0 to the DRAMs.

**2 Gbit** QR DIMMs appear to the host controller logically as Dual Rank 4Gbit DIMMs. The difference between a 2 Gbit part and 4 Gbit parts is the addition of A15 for the Activate Command. The AMB will use Row address A15 in the FBD command as dBA0 to the DRAMs.

For 512 Mbit parts, the dBA0 bit is created from BA2, which is sent for all commands which are rank specific, so this is a simple mapping. For 1 Gbit and 2 Gbit DRAMs, a Row Address is used to create the DRAM dBA0. This bit is ONLY sent during activate commands. This requires the AMB to remember the dBA0 bit from the last activate and use it for subsequent Read, Write, and Precharge Single commands. The DRAM's BA0 essentially becomes a row address in Quad Rank Mode C.

The AMB must store the dBA0 bit separately for each combination of BA2:0 and RS0 from the host controller. This is required because the host could have sent a different dBA0 for each possible open bank. This requires 16 dBA0s to be stored in the AMB, corresponding to the 16 banks that could be open at one time by the host controller. The dBA0 is stored when it is sent with the Activate Command, and used for any subsequent read, write, and precharge command to the same bank of the same logical rank.

On each activate, the AMB stores the value being sent on dBA0 in one of 16 locations selected by the host RS bit and BA[2:0] bits. This represents each different bank that the host controller could consider opened.

One each read, write, or precharge single command the AMB selects the proper stored value by using the RS bit and BA[2:0] bits send by the host in the read, write, or precharge command.

**Table 58 — Activate Command Mapping**

Host (FBD channel) bit	512 Mbit DRAM	1 Gbit DRAM	2 Gbit DRAM	All other modes
BA0	(RS1)	(RS1)	(RS1)	BA0
BA1	BA1	BA1	BA1	BA1
BA2	BA0	BA2	BA2	BA2
A[13:0]	A[13:0]	A[13:0]	A[13:0]	A[13:0]
A14	(A14)	BA0	A14	A14
A15	(not used)	(not used)	BA0	A15
RS	selects ranks	selects ranks	selects ranks	selects ranks

### 13.3.1 Quad Rank Mode C (cont'd)

**Table 59 — Read, Write, and Precharge Single Command Mapping**

Host (FBD channel) bit	512 Mbit DRAM	1 Gbit DRAM	2 Gbit DRAM	All other modes
BA0	(RS1)	(RS1)	(RS1)	BA0
BA1	BA1	BA1	BA1	BA1
BA2	BA0	BA2	BA2	BA2
A[13:0]	A[13:0]	A[13:0]	A[13:0]	A[13:0]
RS	selects ranks	selects ranks	selects ranks	selects ranks
Stored BA0 bit from the activate	(not used)	BA0	BA0	(not used)

**Table 60 — Rank Selection and dBA0 Generation for Each Command Type**

Command	Rank Decoding	DRAM BA0
Activate	Uses Host BA0	512 Mbit: Host BA2 used 1 Gbit: Host A14 used 2 Gbit: Host A15 used
Read	Uses Host BA0	512 Mbit: Host BA2 used For 1 Gbit and 2 Gbit parts this is a stored value from the last activate command to the same bank and rank. Which stored bit is determined by the host BA[2:0] and RS bits. Which stored bit is used is determined by the host BA[2:0] and RS bits
Write	Uses Host BA0	512 Mbit: Host BA2 used For 1 Gbit and 2 Gbit parts this is a stored value from the last activate command to the same bank and rank. Which stored bit is used is determined by the host BA[2:0] and RS bits.
Precharge Single	Uses Host BA0	512 Mbit: Host BA2 used For 1 Gbit and 2 Gbit parts this is a stored value from the last activate command to the same bank and rank. Which stored bit is used is determined by the host BA[2:0] and RS bits.
Auto Refresh	Command is sent to two ranks. RS bit determines whether it is sent to Ranks 0 and 2 or Ranks 1 and 3.	N/A
Precharge All	Command is sent to two ranks. RS bit determines whether it is sent to Ranks 0 and 2 or Ranks 1 and 3.	N/A

**Table 60 — Rank Selection and dBA0 Generation for Each Command Type (Continued)**

Command	Rank Decoding	DRAM BA0
Enter Self Refresh	Command is sent to two ranks. RS bit determines whether it is sent to Ranks 0 and 2 or Ranks 1 and 3.	N/A
Exit Self Refresh / power down	Command is sent to two ranks. RS bit determines whether it is sent to Ranks 0 and 2 or Ranks 1 and 3. Note that this command only involves the CKE signals which are physically shared by Ranks 0 and 2, and by Ranks 1 and 3.	N/A
Enter Power Down	Command is sent to two ranks. RS bit determines whether it is sent to Ranks 0 and 2 or Ranks 1 and 3. Note that this command only involves the CKE signals which are physically shared by Ranks 0 and 2, and by Ranks 1 and 3.	N/A
CKE per DIMM	Sent to all ranks on the DIMM	N/A
CKE per rank	Command is sent to two ranks. The appropriate RS bit determines whether it is sent to Ranks 0 and 2 or Ranks 1 and 3. Note that this command only involves the CKE signals which are physically shared by Ranks 0 and 2, and by Ranks 1 and 3.	N/A

### 13.3.1.1 Host Responsibilities for Read Timing

The host controller is responsible for assuring that there is a turnaround cycle between reads to the same DIMM but different ranks. This includes switching between physical ranks that appear as one logical rank in the Mode C addressing mode.

### 13.3.2 FBD2 Mode A Rank Decode

Mode A uses DS2 (DIMM Select 2) as the additional rank decode. This limits the total number of DIMMs to 4 per channel, as decoded by DS[1:0]. For Mode A, the host controller knows about the 4 individual ranks, and addresses them directly.

The decode for DS[2:0] within the AMB normally comes from the strapping signals SA[2:0], which provides the physical DIMM number, setting the address for the SPD and AMB. This DIMM number is compared to the DS[2:0] in the command frames. In Quad Rank Mode A, a quad rank DIMM decode ignores the DS2 bit, using it as Rank Select 1. By the same token, in Quad Rank Mode A, a quad rank DIMM decode will also ignore the WS2 bit which was used by the AMB on the DIMM to determine if it should write the Wdata into its write FIFO. Single and dual rank DIMMs will continue to decode DS2 as a DIMM select bit.

**Table 61 — Quad Rank Mode A DS[2:0] and RS Mapping**

DIMM Type	DS2 (RS1)	DS1	DS0	RS
Quad Rank DIMM	Rank Select 1	DIMM Decode	DIMM Decode	Rank Select 0
Dual Rank DIMM	DIMM Decode	DIMM Decode	DIMM Decode	Rank Select
Single Rank DIMM	DIMM Decode	DIMM Decode	DIMM Decode	Not Used

### 13.2.2 FBD2 Mode A Rank Decode (cont'd)

In Mode A, the AMB need not store the rank information for each bank, since the rank select is sent with all DRAM commands for all densities.

Operations other than DRAM commands operate in the same manner as a single or dual rank DIMM.

A quad rank DIMM responds to configuration read and write cycles at its selected DIMM number, decoding DS[2:0]. It does not respond to configuration read and write cycles at the alternate address with DS2=1.

A quad rank DIMM sends status frames providing data only on the lane selected by SA[2:0]. It does NOT repeat the status information on the additional lane selected when DS2=1.

The example in Table 62 is for a quad rank DIMM with the strapping of SA[2:0] = 001 (DIMM 1).

**Table 62 — AMB Response to Commands**

Command	AMB response, when SA[2:0]=001
Activate	Responds to DS[2:0]=001 (Ranks 0 and 1)
Write	Responds to DS[2:0]=101 (Ranks 2 and 3)
Read	
Precharge All	Commands are sent to a single rank.
Precharge Single	
Auto Refresh	
Enter Self Refresh	Responds to DS2:0]=x01
Exit Self Refresh/Exit Power Down	Since CKE is shared between ranks 0&2 and ranks 1&3, these commands target 2 ranks at a time, based on the RS bit. RS=0 targets command to ranks 0 and 2. RS=1 targets command to ranks 1 and 3.
Enter Power Down	
Channel commands Config read and write CKE per DIMM CKE per Rank	Responds to DS[2:0]=001 only
Status Packet	Drives data onto logical lane 1 only

### 13.4 ODT Timing on Reads

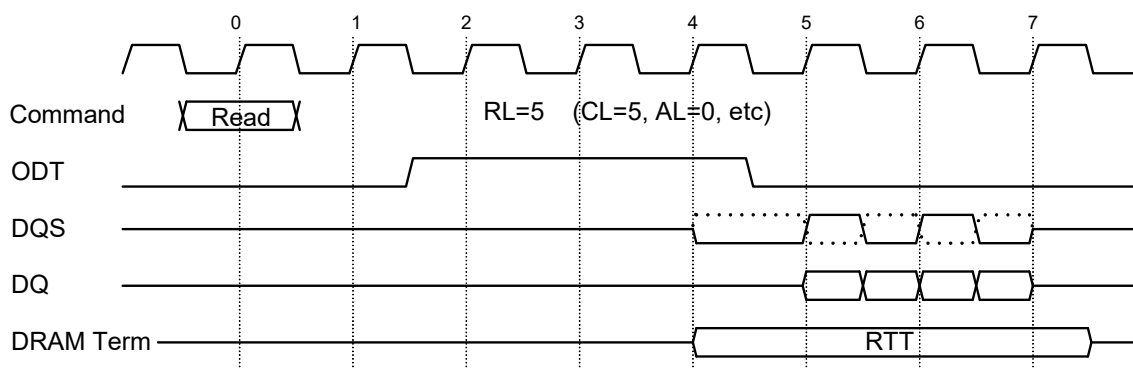
The read timing for ODT is basically the same as the write timing. The ODT is enabled for the DQS preamble, and remains active for 3.5 clocks for BL=4 and 5.5 clocks for BL=8. The equation for the DRAM ODT signals is:

Turn on: RL - 3 clocks from the read command

Turn off: RL - 2 + (BL/2) clocks from the read command



### 13.4 ODT Timing on Reads (cont'd)



**Table 63 — DRAM ODT Timing during Reads**

#### 13.4.1 AMB Data Bus Termination

The AMB data bus termination remains at 65 ohms nominal.

### 13.5 Registers

DDR2ODTC: DDR2 DRAM On-Die Termination Control

Note: This is an existing register, in which previously only 8 bits were used. In reality, since the AMB only has one ODT pin set for ranks 0 and rank 1, only 4 of the 8 bits have any function. These original 8 bits are not changed.

For the quad rank option using 4 ODT signals, 8 more bits are added for control of the ODT1 and ODT2 signals for reads. There is one bit for each rank reads.

**Registers Table**

Device: NodeID Function: 4 Offset: FCh			
Bit	Attr	Default	Description
15	RWST	0	ODT2 control during reads from CS3
14	RWST	0	ODT1 control during reads from CS3
13	RWST	0	ODT2 control during reads from CS2
12	RWST	0	ODT1 control during reads from CS2
11	RWST	0	ODT2 control during reads from CS1
10	RWST	0	ODT1 control during reads from CS1
9	RWST	0	ODT2 control during reads from CS0
8	RWST	0	ODT1 control during reads from CS0 1: ODT pin will drive high 0: ODT pin will drive low

**Registers Table (Continued)**

<b>Device: NodeID</b> <b>Function: 4</b> <b>Offset: FCh</b>			
Bit	Attr	Default	Description
Note that bits 7:0 below do not change from the current spec			
7:6	RWST	0h	R1ODTWR: ODT control during writes to CS1 & CS3 x1: ODT0A/B, ODT1, & ODT2 pins will drive high x0: ODT0A/B, ODT1, & ODT2 pins will drive low Note: Must always be set to 01 for SR and DR DIMMs
5:4	RWST	0h	R1ODTRD: ODT0 control during reads to CS1 & CS3 x1: ODT0A/B pins will drive high x0: ODT0A/B pins will drive low Note: Must always be set to 00
3:2	RWST	0h	R0ODTWR: ODT control during writes to CS0 & CS2 x1: ODT0A/B, ODT1, & ODT2 pins will drive high x0: ODT0A/B, ODT1, & ODT2 pins will drive low Note: Must always be set to 01 for SR and DR DIMMs
1:0	RWST	0h	R0ODTRD: ODT0 control during reads to CS0 & CS2 x1: ODT0A/B pins will drive high x0: ODT0A/B pins will drive low Note: Must always be set to 00

Quad Rank control register

**Quad Rank Control Register Table**

<b>Device: NodeID</b> <b>Function: 3</b> <b>Offset: 88h</b>			
Bit	Attr	Default	Description
5	RWST	0	A15A and A15B pin muxing 0 = A15A and A15B functionality 1 = ECCA2 and ECCA6 functionality. Only permitted when the Quad Rank Enable bit is set to a 1.
4	RWST	0	CKE0B and CKE1B pin muxing 0 = CKE0B and CKE1B functionality 1 = ODT1 and ODT2 functionality. Only permitted when the Quad Rank Enable bit is set to a 1.

**Quad Rank Control Register Table (Continued)**

<b>Device: NodeID</b> <b>Function: 3</b> <b>Offset: 88h</b>			
Bit	Attr	Default	Description
3:2	RWST	00	RS1 Select. This field determines what the AMB uses for the dBA0 (DRAM BA0) 00 = BA2 used for dBA0 01 = Row Address 14 used for dBA0 10 = Row Address 15 used for dBA0 11 = DS2 (Quad Rank Mode A)
1			Reserved
0	RWST	0	Quad Rank Enable 0 = normal single or dual rank operation 1 = Quad Rank DIMM

DCALCSR

Bits 23 and 24 added to support the additional ranks.

<b>Device: NodeID</b> <b>Function: 4</b> <b>Offset: 40h</b>			
Bit	Attr	Default	Description
24:21	RW	0000	This field corresponds to the chip select outputs: CS[3:0]. Setting a bit in this field will cause the corresponding CS pin to drive low when commands are issued on the DDR bus. This field Applies to NOP, Refresh, Precharge all, and MRS/EMRS commands. Bit 21 is for CS0, Bit 22 if for CS1, Bit 23 is for CS2, and bit 24 is for CS3.

DCALADDR: DCAL Address Register

Bits 5:4 are added to XOR with ECCA2 and ECCA6

**DCALADDR: DCAL Address Register Table**

<b>Device: NodeID</b> <b>Function: 4</b> <b>Offset: 44h</b>	
Bit	Description
31:16	DRAM Address Bus 15:0
15:6	Reserved
5	XOR for ECCA6. This bit is set to a 1 to have the ECC A6 bit the opposite of A6. Only used if quad rank and A15A/B pin muxing enabled (function 3 offset 0x88 bits 0 and 5), otherwise ignored.

**DCALADDR: DCAL Address Register Table (Continued)**

<b>Device: NodeID</b> <b>Function: 4</b> <b>Offset: 44h</b>	
Bit	Description
4	XOR for ECCA2. This bit is set to a 1 to have the ECC A2 bit the opposite of A2. Only used if quad rank and A15A/B pin muxing enabled (function 3 offset 0x88 bits 0 and 5), otherwise ignored.
3	Reserved
2:0	DRAM Bank Address bus 2:0

Shaded rows are unchanged.

A6/A2 and ECCA6/ECCA2 functionality of DCALADDR if Quad rank mode and A15A/B pin muxing enabled (function 3 offset 0x88 bits 0 and 5).

Signal	DCALADDR Bits
A6A, A6B	Bit 22 (existing definition)
ECCA6	Bit 22 XOR Bit 5
A2A, A2B	Bit 18 (existing definition)
ECCA2	Bit 18 XOR Bit 4

MEMBIST register change

Only the two bits within the register that change are shown. Changes are shown in bold.

<b>Device: NodeID</b> <b>Function: 3</b> <b>Offset: 40h</b>			
Bit	Attr	Default	Description
21:20	RW	00	CS: CS[3:0] selection in MemBIST mode 01: Select Rank 0 10: Select Rank 1 00: Select Rank 2 11: Select Rank 3

Note that the encoding of this register is based on the existing definition.

### 13.6 Fast Reset

During a fast reset, the AMB performs a set of operations to close all pages and put the DRAMs into self refresh. The AMB will access two ranks in parallel for all commands during this time.

Note that for QRx8 this will be activating the same number of DRAMs at a time as is already done for DRx4 DIMMs.

For Quad Rank FB-DIMM MEMBIST and Transparent Mode support, please refer to [JESD82-28A “Fully Buffered DIMM Design for Test, Design for Validation \(DFx\)”](#).

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**Annex A - (Informative) Difference between JESD82-20A.01 and JESD82-20A**

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Editorial revisions as follows:

1. Changed “master” to “controller” in the following clauses:
  - Level 2 clause 1.6 - Glossary, definition of SMBus
  - Level 2 clause 7.1
  - Level 3 clauses 1.4.3, 7.1.1, 7.1.2, 7.1.3, and 7.1.4
  - Level 4 clauses 7.1.3.1, 7.1.3.2, 7.1.5.1, 7.1.5.2, and 7.1.5.3
  - Tables in Level 4 clauses 11.8.1.1 and 11.8.2.1
2. Changed “slave” to “target” in the following clauses:
  - Level 2 clauses 2.6 and 7.1
  - Level 3 clause 1.4.3, 7.1.2, and 7.1.4
  - Level 4 clauses 7.1.3.2, 7.1.5.1, and 7.1.5.2
  - Tables in Level 4 clauses 11.8.1.1 and 11.8.2.1
3. Changed Table captions, Figure captions, and headings to Initial Caps
4. Formatted all tables to the JEDEC standard layout

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**Standard Improvement Form****JEDEC Standard JESD82-20A.01**

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1. I recommend changes to the following:

☐ Requirement, clause number \_\_\_\_\_

☐ Test method number \_\_\_\_\_ Clause number \_\_\_\_\_

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other \_\_\_\_\_

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2. Recommendations for correction:


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3. Other suggestions for document improvement:


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